BASIC ELECTRONICS LAB MANUAL

B.Tech (ECE)

COURSE CODE: EC191

DEPARTMENT OF ELECTRONICS & COMMUNICATION

Introduction

There are 3 periods allocated to a laboratory session in Digital Electronics. It is a necessary part of the course at which attendance is compulsory.

Here are some guidelines to help you perform the experiments and to submit the reports:

1. *Read all instructions carefully and carry them all out.*
2. *Ask a demonstrator if you are unsure of anything.*
3. *Record actual results (comment on them if they are unexpected!)*
4. *Write up full and suitable conclusions for each experiment.*
5. *If you have any doubt about the safety of any procedure, contact the demonstrator beforehand.*
6. *THINK about what you are doing!*

SYLLABUS

Basic Electrical and Electronics Engineering-I
Code : ES191
Contacts:
Credits : 2

Basic Electronics Engineering Laboratory - I

- *There will be a couple of familiarization lectures before the practical classes are undertaken where basic concept of the instruments handled Egg: CRO, Multimeters etc will be given. Lectures on measurement techniques and error calculation will also have to be organized.*
- *3 hours per week must be kept, initially for practical lectures, and later for tutorials.*

List of Experiments :

1. Familiarisation with passive and active electronic components such as Resistors, Inductors, Capacitors, Diodes, Transistors (BJT) and electronic equipment like DC power supply,multimeters etc.
2. Familiarization with measuring and testing equipment like CRO, Signal generators etc.
3. Study of I-V characteristics of Junction diodes.
4. Study of I-V characteristics of Zener diodes.
5. Study of Half and Full wave rectifiers with Regulation and Ripple factors.
6. Study of I-V characteristics of BJTs.

INTRODUCTION -1

AIM: Familiarisation with passive and active electronic components.

What is electronics components?

Electronic components have a number of electrical terminals or leads. These leads connect to other electrical components, often over wire, to create an electronic circuit with a particular function (for example an amplifier, radio receiver, or oscillator). Basic electronic components may be packaged discretely, as arrays or networks of like components, or integrated inside of packages such as semiconductor integrated circuits, hybrid integrated circuits, or thick film devices. The following list of electronic components focuses on the discrete version of these components, treating such packages as components in their own right.

Components can be classified as

I) Passive components,

II) Active components

PASSIVE COMPONENTS

These types of components cannot use mesh energy into the electronic circuit because they don't rely on a power source, excluding what is accessible from the AC circuit they are allied to. As a result, they cannot amplify, although they can increase a current otherwise voltage or current. These components mainly include two-terminals like resistors, inductors, transformers & capacitors

ACTIVE COMPONENT

These components are used to amplify electrical signals to generate electric power. The functioning of these components can be done like an AC circuit within electronic devices to protect from voltage and enhanced power. An active component executes its functions because it is power-driven through an electricity source. All these components require some energy source that is normally removed from a DC circuit. Any quality type of active component will include an oscillator, IC (integrated circuit) &

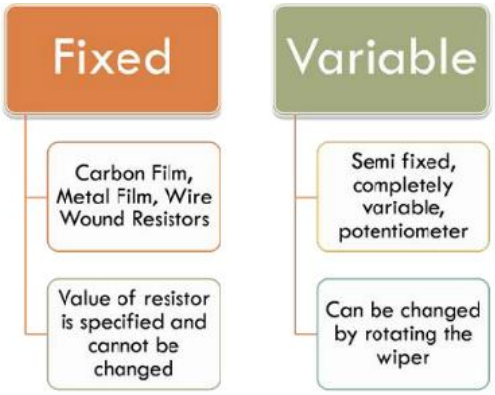
AIM:

- Measure the value of a Resistor, Capacitor.
- Measure the Tolerance of a Resistor.
- Explain the types of Resistors, Capacitor.

What is resistor?

Pass current in proportion to voltage (Ohm's law) and oppose current.

Types of Resistors



Carbon Film Resistors:

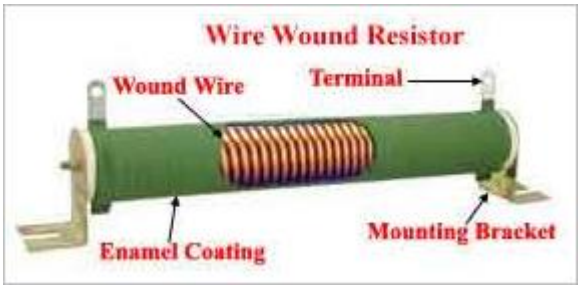
- Most general purpose ,cheap resistor
- Tolerance of Resistance value is usually +/- 5%
- Power ratings of 1/8 W ,1/4 W and ½ W are usually used .

Metal Film Resistor

- Used when higher tolerance is needed , ie more value.
- They have about +/- 0.05% tolerance

Wire Wound Resistors:

- A wire wound resistor is made of metal resistance wire, and because of this they can be manufactured to precise values
- Also, high wattage resistors can be made by thick wire material
- Wire wound resistors in a ceramic case are called as ceramic resistors
- Wire wound resistors in a ceramic case are called as ceramic resistors



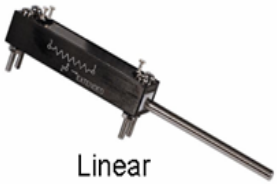
Variable resistors

Shaft Potentiometer

Precision Shaft Potentiometer

Trim Potentiometer

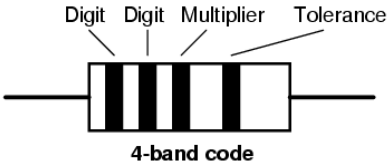
Slide Potentiometer



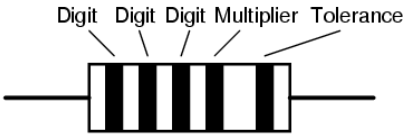
Linear Potentiometer

Hollow Shaft Potentiometer

Reading Value of Fixed Resistors::

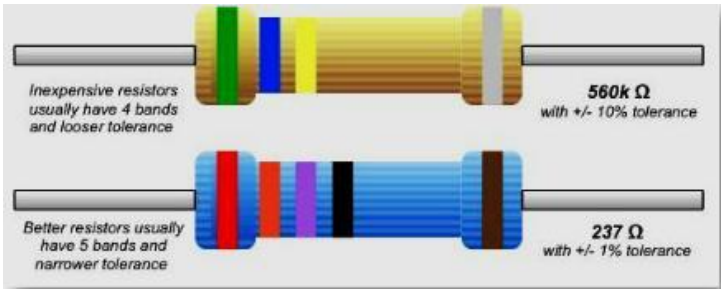


4-band code

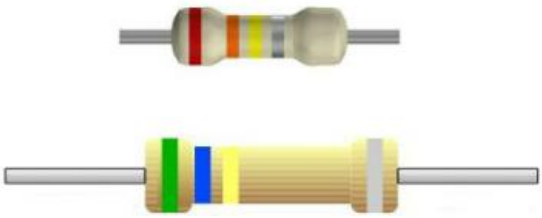


5-band code

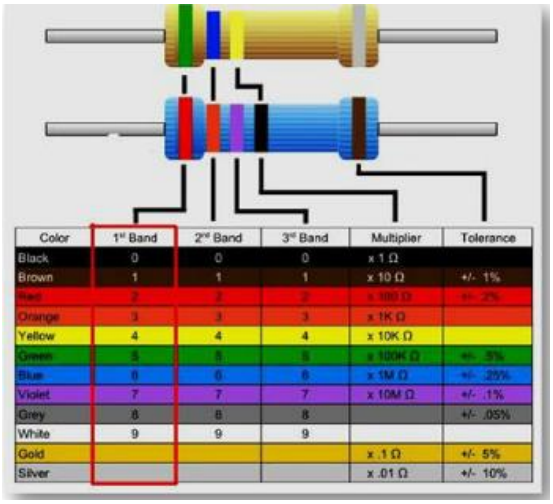
- Resistors are colour coded as they are too small for the value to be written on them.
- There are 4 or 5 bands of colour . Value of a Resistor is decoded from these band of colours.



- If your resistor has four colour bands ,turn the resistor so that the gold or silver band is on right hand side or the end with more bands should point left.

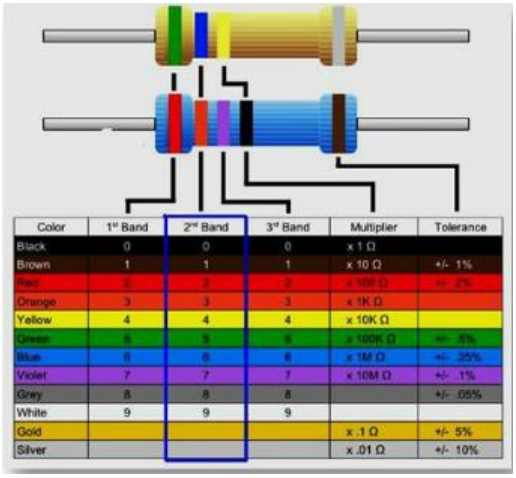


The first band is now on the left hand side. This represents the first digit .Based on the colour make a note of the digit .In this case- 4 band its '5' and for 5 band its '2'.



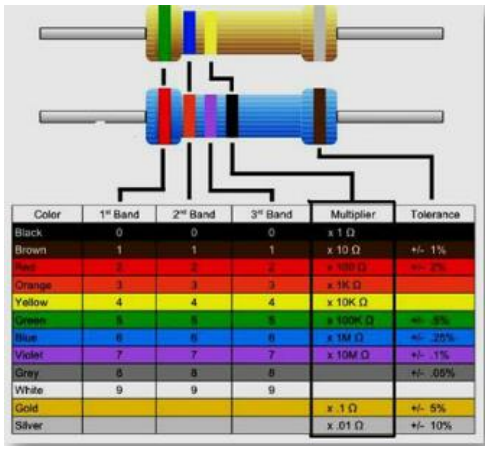
Color	1st Band	2nd Band	3rd Band	Multiplier	Tolerance
Black	0	0	0	x 1 Ω	
Brown	1	1	1	x 10 Ω	+/- 1%
Red	2	2	2	x 100 Ω	+/- 2%
Orange	3	3	3	x 1K Ω	
Yellow	4	4	4	x 10K Ω	
Green	5	5	5	x 100K Ω	+/- .5%
Blue	6	6	6	x 1M Ω	+/- .25%
Violet	7	7	7	x 10M Ω	+/- .1%
Grey	8	8	8		+/- .05%
White	9	9	9		
Gold				x .1 Ω	+/- 5%
Silver				x .01 Ω	+/- 10%

The second band represents the second digit. The colours represent the same numbers as did the first digit .In this case –4 band its'6' and for 5 band its'3'.



Color	1st Band	2nd Band	3rd Band	Multiplier	Tolerance
Black	0	0	0	x 1 Ω	
Brown	1	1	1	x 10 Ω	+/- 1%
Red	2	2	2	x 100 Ω	+/- 2%
Orange	3	3	3	x 1K Ω	
Yellow	4	4	4	x 10K Ω	
Green	5	5	5	x 100K Ω	+/- .5%
Blue	6	6	6	x 1M Ω	+/- .25%
Violet	7	7	7	x 10M Ω	+/- .1%
Grey	8	8	8		+/- .05%
White	9	9	9		
Gold				x .1 Ω	+/- 5%
Silver				x .01 Ω	+/- 10%

The third band divulges how many zeros to add/divide to the first two numbers –for a 4 band Resistor . In this case – 4 band its '4' zeroes to be added . So value is 560K.



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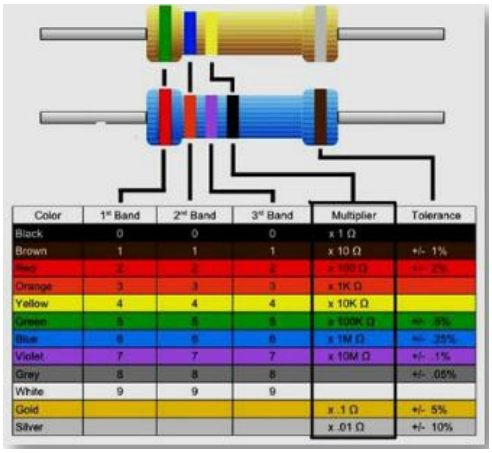
Orange	3	3	3	x 1K Ω	
Yellow	4	4	4	x 10K Ω	
Green	5	5	5	x 100K Ω	+/- .5%
Blue	6	6	6	x 1M Ω	+/- .25%
Violet	7	7	7	x 10M Ω	+/- .1%
Grey	8	8	8		+/- .05%
White	9	9	9		
Gold				x .1 Ω	+/- 5%
Silver				x .01 Ω	+/- 10%

The third band denotes the 3rd digit – for a 5 band Resistor. In this case –5 band its '7' . So the value of the 5 band resistor is 237 Ohms as its multiplier digit is '0.



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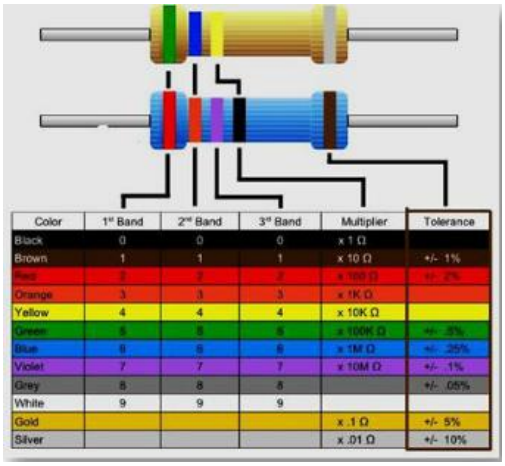
Red	2	2	2	x 100 Ω	+/- 2%
Orange	3	3	3	x 1K Ω	
Yellow	4	4	4	x 10K Ω	
Green	5	5	5	x 100K Ω	+/- .5%
Blue	6	6	6	x 1M Ω	+/- .25%
Violet	7	7	7	x 10M Ω	+/- .1%
Grey	8	8	8		+/- .05%
White	9	9	9		
Gold				x .1 Ω	+/- 5%
Silver				x .01 Ω	+/- 10%

The last band denotes the tolerance. So the value of the 4 band resistor it is +/- 10% while for the 5 band resistor it is +/- 1%.



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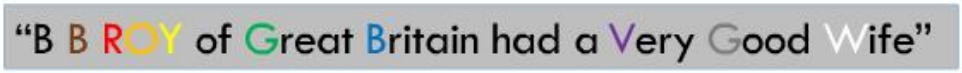
Green	5	5	5	x 100K Ω	+/- .5%
Blue	6	6	6	x 1M Ω	+/- .25%
Violet	7	7	7	x 10M Ω	+/- .1%
Grey	8	8	8		+/- .05%
White	9	9	9		
Gold				x .1 Ω	+/- 5%
Silver				x .01 Ω	+/- 10%

- Tolerance of a Resistor is also an important property to consider .
- A 100 ohm resistor with a 10 % tolerance can mean its value can be any fixed value between 90 to 110 Ohms.

- A 120 Ohm resistor with a 10 % tolerance can mean its value can be any fixed value between 108 and 132 Ohms.

Mnemonic to Remember

Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9
Gold	



Color	Digit	Multiplier	Tolerance (%)
Black	0	10^0 (1)	
Brown	1	10^1	1
Red	2	10^2	2
Orange	3	10^3	
Yellow	4	10^4	
Green	5	10^5	0.5
Blue	6	10^6	0.25
Violet	7	10^7	0.1
Grey	8	10^8	
White	9	10^9	
Gold		10^{-1}	5
Silver		10^{-2}	10
(none)			20

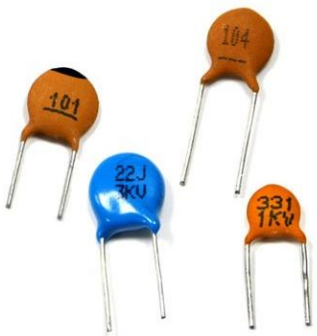
What is Capacitor?

It is one of the passive components like resistor. Capacitor is also known as condenser. Capacitor is generally used to store the charge. The charge is stored in the form of "electrical field". Capacitors play a major role in many electrical and electronic circuits.

Classification of Capacitors

UN-POLARIZED	POLARIZED
Ceramic	Electrolytic
Multilayer	Tantalum
Polystyrene Film	Super
Polyster Film	They have positive and negative electrode
Polypropylene	
Mica	
They don't have positive and negative electrode	

Ceramic Capacitors:



Ceramic capacitors are the most used capacitors in the electronics industry. Ceramic capacitors are fixed capacitance type capacitors and they are usually very small (in terms of both physical dimensions and capacitance). The capacitance of ceramic capacitors is usually in the range of pico farads to few micro farads (less than 10μF). They are non-polarised type capacitors and hence can be used in both DC as well as AC circuits

.

Electrolytic Capacitor

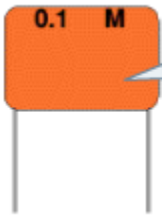
Electrolytic capacitors are polarized and they must be connected the correct way round , at least one of their leads will be marked + or – . It is very easy to find the

values of electrolytic capacitors because they are clearly printed with their capacitance and voltage rating.

Tantalum Capacitor:

Tantalum bead capacitors are polarized and have low voltage ratings like electrolytic capacitors . Usually , the "+" symbol is used to show the positive component lead . Modern tantalum bead capacitors are printed with their capacitance voltage and polarity in full. However older ones use a colour – code systems which has two stripes (for the two digits) and a spot of colour for the number of zeros to give the value in fun.

Un-polarized Capacitors- small values(up to 1uF)



The value printed but without a multiplier, so you need to use experience to work out what the multiplier should be! For example 0.1 means 0.1 pF. Sometimes the multiplier is used in place of the decimal point: For example: 4n7 means 4.7n

Un-polarized Capacitors — Capacitor Number Code

A number code is often used on small capacitors where printing is difficult: The 1st number is the 1st digit, the 2nd number is the 2nd digit, the 3rd number is the number of zeros to give the capacitance in pF. Ignore any letters - they just indicate tolerance and voltage rating. For example: 102 means 1000pF (not 102pF!) For example: 472J means 4700pF (J means 5% tolerance).

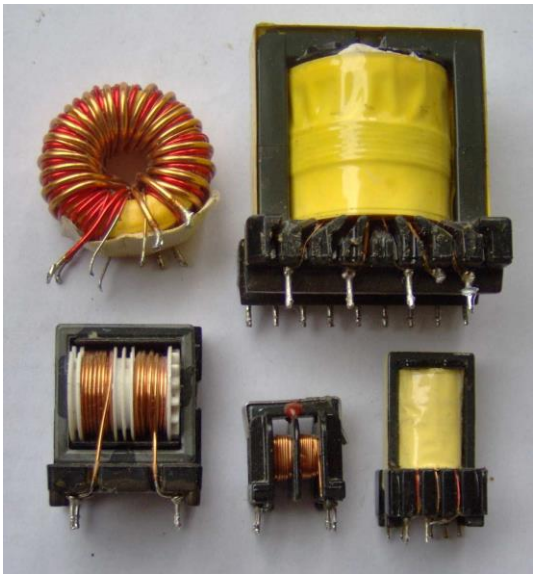
Un-polarized Capacitors — Capacitor Colour Code

Structure of an Inductor

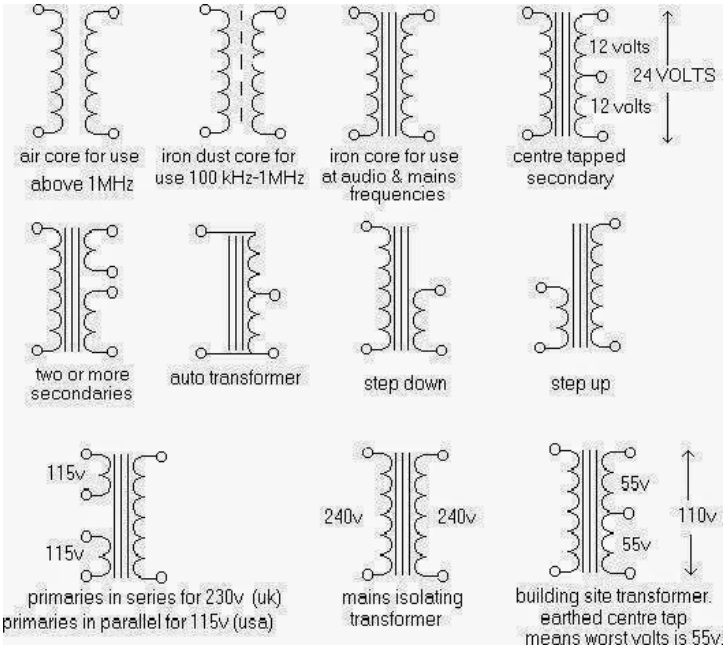
Inductance

1. No of turns of wire wound around the coil
2. Cross sectional area of the coil
3. The material type of the coil
4. The Length of the coil

Transformers



Various transformers

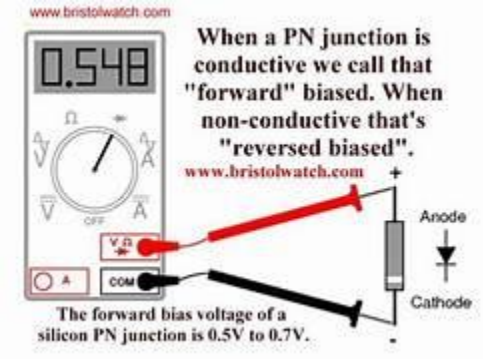


INTRODUCTION-2

AIM:

Familiarization with measuring and testing equipment like CRO, Signal generators etc.

Digital Multimeter



The Breadboard

The breadboard consists of two terminal strips and two bus strips (often broken in the centre). Each bus strip has two rows of contacts. Each of the two rows of contacts are a node. That is, each contact along a row on a bus strip is connected together (inside the breadboard). Bus strips are used primarily for power supply connections, but are also used for any node requiring a large number of connections. Each terminal strip has 60 rows and5 columns of contacts on each side of the centre gap. Each row of 5 contactsis a node.You will build your circuits on the terminal strips by inserting the leads ofcircuit components into the contact receptacles and making connections with22-26 gauge wire. There are wire cutter/strippers and a spool of wire in thelab. It is a good practice to wire +5V and 0V power supply connections toseparate bus strips.

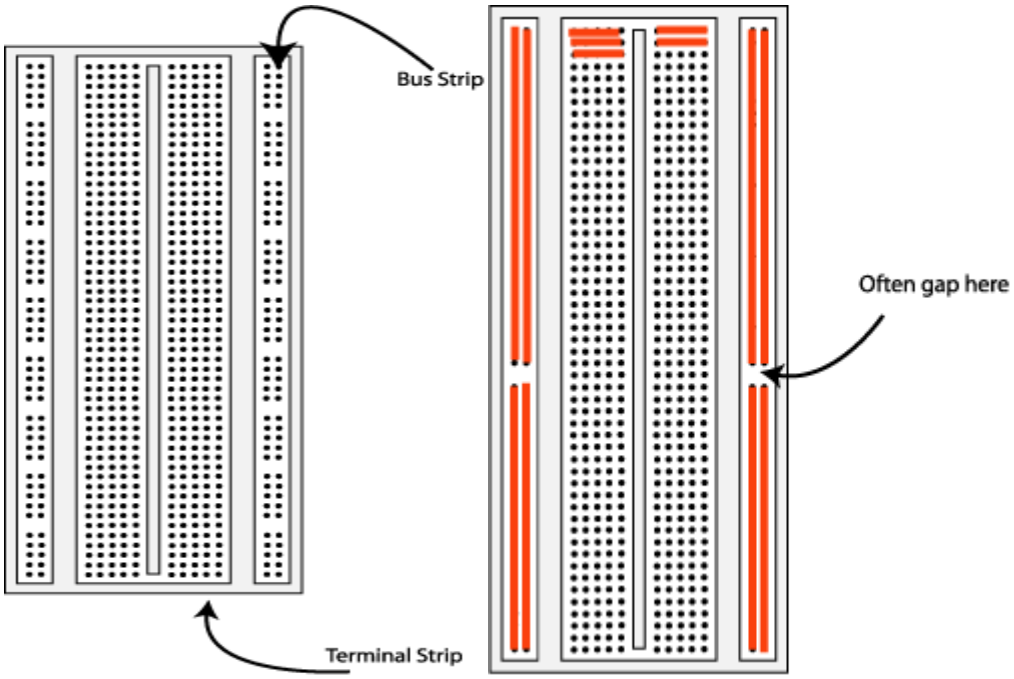
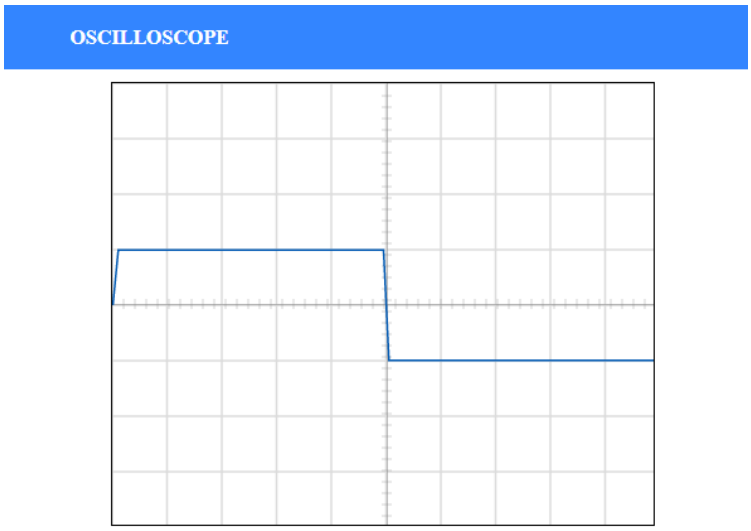


Fig 1. The breadboard. The lines indicate connected holes.

CATHODE RAY TUBE

The screen is cathode ray tube found in most television sets where the face of the screen is divided up into a 2 dimensional grid (or axes or scale); In this experiment we consider 8x10 grid. The vertical grid is divided up into 8 (major) divisions and the horizontal grid is divided into 10 major divisions. To improve the precision, each of these divisions is further broken up into 5 minor divisions. The horizontal axis (X-axis) represents time and the vertical axis (Y-axis) represents voltage. The scope displays (also called a signal trace or trace) the input signal voltage along the vertical (or Y-axis) while an internally generated signal (called the horizontal sweep or sweep signal) is simultaneously produced along the X-axis creating a 2- dimensional time trace of the input signal.



volts/div*- This control lets you change how many volts are represented by each vertical increment of grid (vertical axis) on the screen. Basically, it allows you to zoom in and out along the y axis.*

time/div- *This control lets you change how much time is represented by each horizontal increment of the grid overlay on the screen. It allows you to zoom in and out along the x axis.*

If volt/div is set to 1 volt which implies each major vertical division is 1 volt where as each minor vertical division is 0.2 volt. And time/div is set to 0.1ms/div which implies each major horizontal division is 0.1ms. Voltage on the vertical scale is 1 volt/div multiply by (number of division). Time on the horizontal scale is 0.1msec multiply by (number of division). In the figure 2, 1 volt/div and amplitude of the input signal is 1 volt. Here 0.1mses/div, the frequency is 1 kHz and its period is 1 complete cycle in 1m sec.if volt/div is set to 2volt/div, which implies each major division is 2 volt where as each minor division is 0.5volt.

Note: If you set the Volts/Div too low, you'll clip the signal. Similarly, setting it too high, and you'll won't find the signal, i.e. the signal will b flat. Increasing the Timebase will display more cycles of a periodic signal. Conversely, reducing the Timebase, fewer cycles will be displayed.

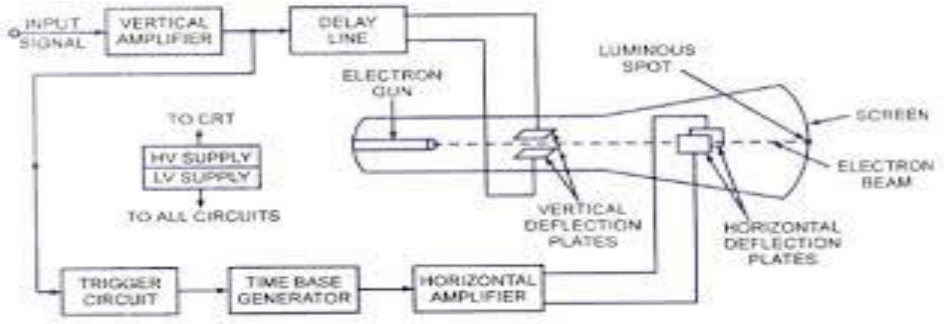
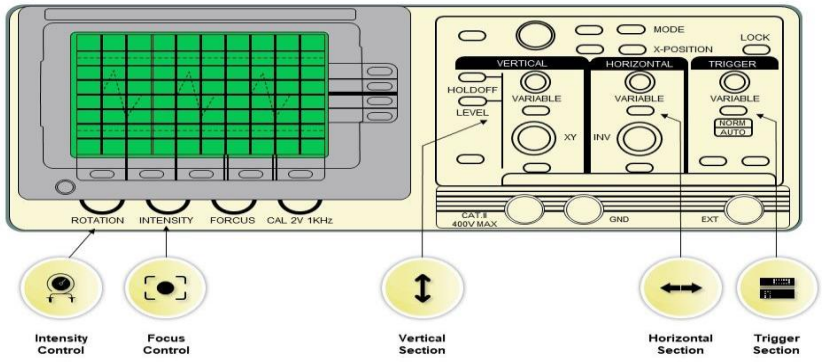


Figure - Block Diagram of General Purpose CRO

Front Panel Control of Cathode Ray Oscilloscope (CRO)

This slide is 100% editable. Adapt it to your needs and capture your audience's attention.



DC power supply

A regulated power supply is an embedded circuit; it converts unregulated AC (Alternating Current) into a constant DC. With the help of a rectifier it converts AC supply into DC. Its function is to supply a stable voltage (or less often current), to a circuit or device that must be operated within certain power supply limits. The output from the regulated power supply may be alternating or unidirectional, but is nearly always DC (Direct Current).[1] The type of stabilization used may be restricted to ensuring that the output remains within certain limits under various load conditions, or it may also include compensation for variations in its own supply source. The latter is much more common today.

Signal generator

A signal generator is one of a class of electronic devices that generates electronic signals with set properties of amplitude, frequency, and wave shape. These generated signals are used as a stimulus for electronic measurements, typically used in designing, testing, troubleshooting, and repairing electronic or electroacoustic devices, though it often has artistic uses as well.There are many different types of signal generators with different purposes and applications and at varying levels of expense. These types include function generators, RF and microwave signal generators, pitch generators, arbitrary waveform generators, digital pattern generators, and frequency generators. In general, no device is suitable for all possible applications.

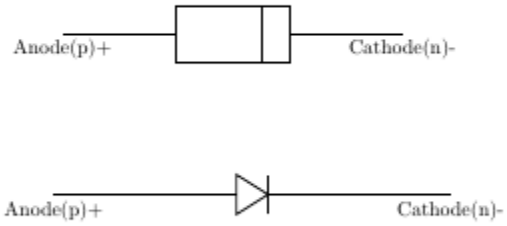
Experiment-1

AIM: *Study the V-I characteristics of a p-n junction diode.*

Component used:

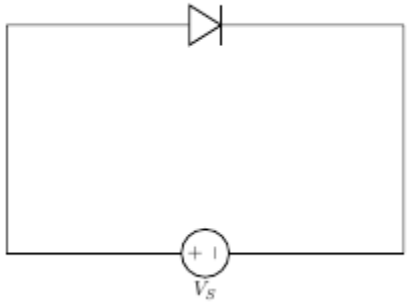
1. IN4007
2. Bread Board
3. Power supply
4. DMM
5. Connecting wire

The diode is a device formed from a junction of n-type and p-type semiconductor material. The lead connected to the p-type material is called the anode and the lead connected to the n-type material is the cathode. In general, the cathode of a diode is marked by a solid line on the diode.

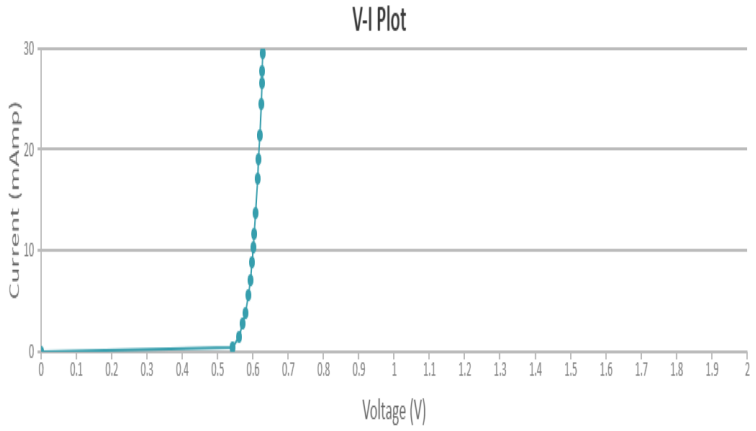


THEORY:

The positive terminal of battery is connected to the P side (anode) and the negative terminal of battery is connected to the N side (cathode) of a diode, the holes in the p-type region and the electrons in the n-type region are pushed toward the junction and start to neutralize the depletion zone, reducing its width. The positive potential applied to the p-type material repels the holes, while the negative potential applied to the n-type material repels the electrons. The change in potential between the p side and the n side decreases or switches sign. With increasing forward-bias voltage, the depletion zone eventually becomes thin enough that the zone's electric field cannot counteract charge carrier motion across the p–n junction, which as a consequence reduces electrical resistance. The electrons that cross the p–n junction into the p-type material (or holes that cross into the n-type material) will diffuse into the nearby neutral region. The amount of minority diffusion in the near-neutral zones determines the amount of current that may flow through the diode.



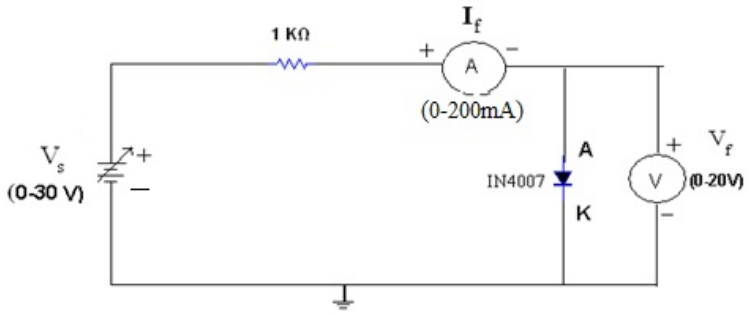
In forward biasing, the positive terminal of battery is connected to the P side and the negative terminal of battery is connected to the N side of the diode. Diode will conduct in forward biasing because the forward biasing will decrease the depletion region width and overcome the barrier potential. In order to conduct, the forward biasing voltage should be greater than the barrier potential. During forward biasing the diode acts like a closed switch with a potential drop of nearly 0.6 V across it for a silicon diode. The forward and reverse bias characteristics of a silicon diode. From the graph, you may notice that the diode starts conducting when the forward bias voltage exceeds around 0.6 volts (for Si diode). This voltage is called cut-in voltage.



Procedure

1. Set DC voltage to 0.2 V .
2. Select the diode.
3. Set the resistor.
4. Voltmeter is placed parallel to Silicon diode and ammeter series with resistor.
5. The positive side of battery to the P side (anode) and the negative of battery to the N side (cathode) of the diode.
6. Now vary the voltage up to 5V and note the Voltmeter and Ammeter reading for particular DC voltage .
7. Take the readings and note Voltmeter reading across Silicon diode and Ammeter reading.

8. Plot the V-I graph and observe the change.
9. Calculate the dynamic resistance of the diode. rd.=ΔV/ΔI
10. Therefore from the graph we see that the diode starts conducting when the forward bias voltage exceeds around 0.6 volts (for Si diode). This voltage is called cut-in voltage.



OBSERVATION TABLE

Serial No.	Forward Voltage(Volt)	Forward Current(m - Amp)

Experiment-2

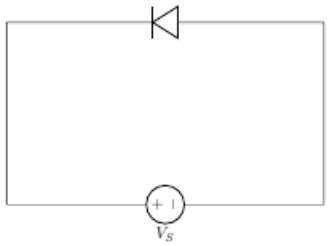
AIM: ***Study of I-V characteristics of Zener diodes.***

Component used:

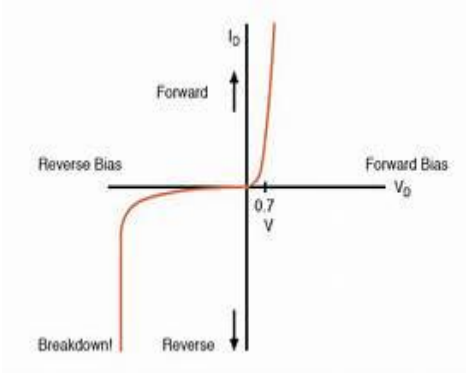
1. Zenger diode
2. Bread Board
3. Power supply
4. Connecting wire
6. DMM

THEORY:

In reverse biasing, the positive terminal of battery is connected to the N side and the negative terminal of battery is connected to the P side of a diode. In reverse biasing, the diode does not conduct electricity, since reverse biasing leads to an increase in the depletion region width; hence current carrier charges find it more difficult to overcome the barrier potential. The diode will act like an open switch and there is no current flow.



When a diode is reverse biased a leakage current flows through the device. This current can be effectively ignored as long as the reverse breakdown voltage of the diode is not exceeded. At potentials greater than the reverse breakdown voltage, charge is pulled through the p-n junction by the strong electric fields in the device and large reverse current flows. This usually destroys the device. There are special diodes that are designed to operate in breakdown. Such diodes are called ***sneer diodes and used as voltage regulators.***



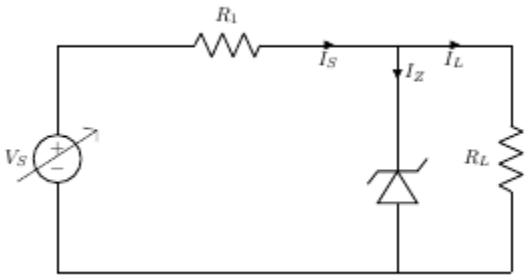
Zener Diode As A Voltage Regulator

A voltage regulator is an electronic circuit that provides a stable DC voltage independent of the load current, temperature and AC line voltage variations. A Zener diode of break down voltage \(V_Z\) is reverse connected to an input voltage source \(V_I\) across a load resistance \(R_L\) and a series resistor \(R_S\). The voltage across the zener will remain steady at its break down voltage \(V_Z\) for all the values of zener current \(I_Z\) as long as the current remains in the break down region. Hence a regulated DC output voltage \(V_0 = V_Z\) is obtained across \(R_L\), whenever the input voltage remains within a minimum and maximum voltage. Basically there are two type of regulations such as:

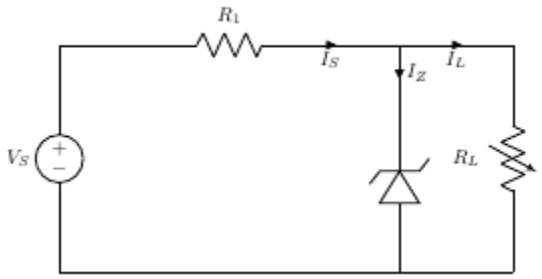
Line Regulation: In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.

Load Regulation: In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.

Line Regulation



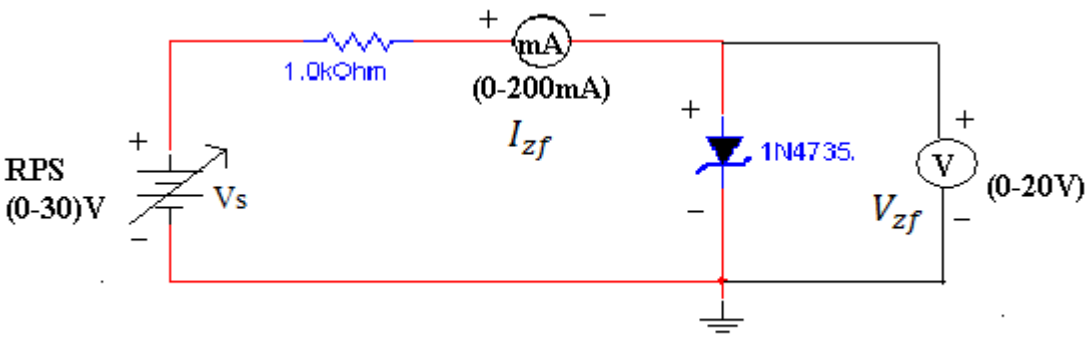
Load Regulation



Procedure

Reverse Bias-Diode

1. Set DC voltage to 0.2 V .
2. Select the diode.
3. Set the resistor.
4. Voltmeter is placed parallel to diode and ammeter series with resistor.
5. The positive side of battery to the P side(anode) and the negative of battery to the N side(cathode) of the diode.
6. Now vary the voltage upto 5V and note the Voltmeter and Ammeter reading for particular DC voltage .
7. Take the readings and note Voltmeter reading across diode and Ammeter reading.
8. Plot the V-I graph and observe the change.



OBSERVATION TABLE

Serial No.	Reverse Voltage(Volt)	Reverse Current(mAmp)

OBSERVATION TABLE (Line Regulation)

Serial No.	Supply Voltage(Volt)	Diode Voltage(Volt)

Experiment-3

AIM: Study thewave form of half wave and full wave rectifier and determine its ripple factor.

Component used:

1.IN4007

2.Bread Board

3.Transformer

4.Connecting wire

6.DMM

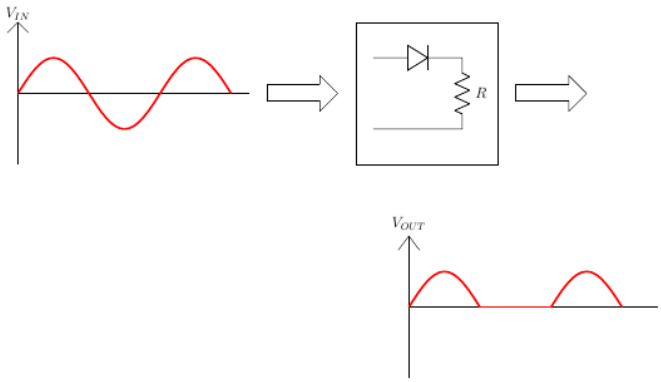
7. Capacitor

8. Resistor

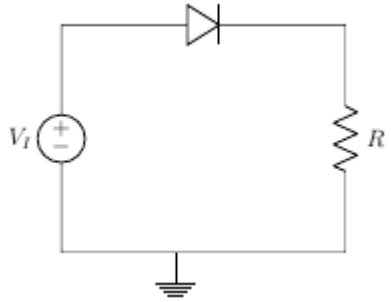
Rectification

A rectifier is a device that converts alternating current (AC) to direct current (DC), a process known as rectification. Rectifiers are essentially of two types – a half wave rectifier and a full wave rectifier.

Half Wave Rectification

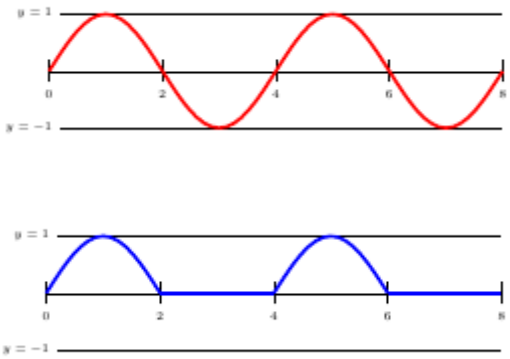


On the positive cycle the diode is forward biased and on the negative cycle the diode is reverse biased. By using a diode we have converted an AC source into a pulsating DC source. In summary we have 'rectified' the AC signal.

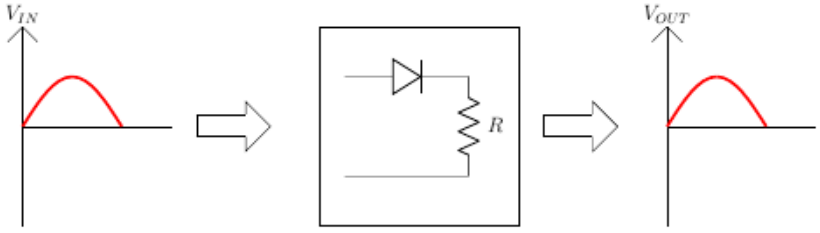


The simplest kind of rectifier circuit is the half-wave rectifier .The half-wave rectifier is a circuit that allows only part of an input signal to pass. The circuit is simply the combination of a single diode in series with a resistor, where the resistor is acting as a load.

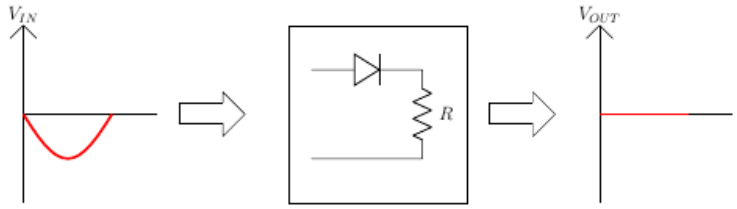
Half Wave Rectifiers – Waveforms



Half Wave Rectification: For Positive Half Cycle

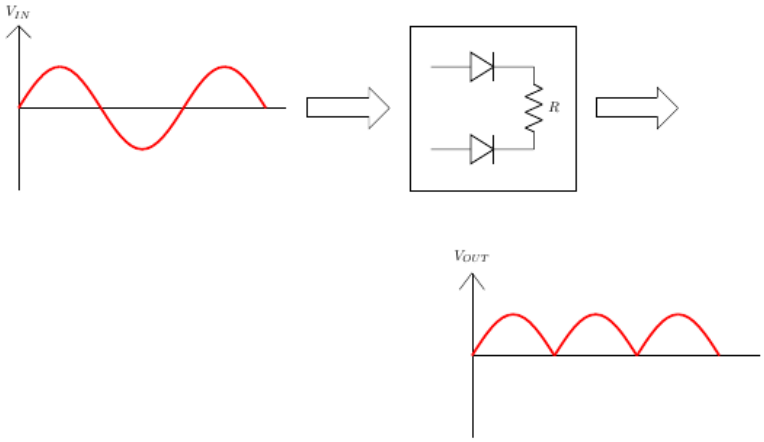


Half Wave Rectification: For Negative Half Cycle

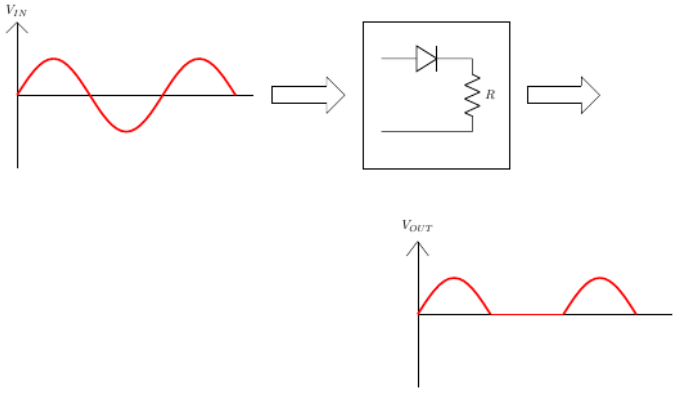


Full Wave Rectifier

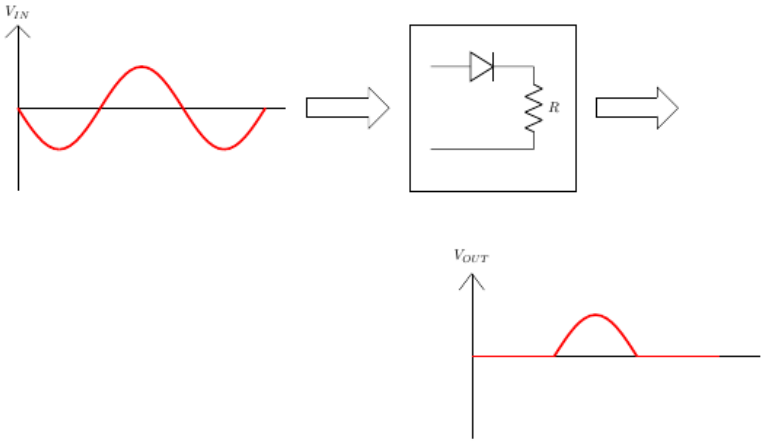
A full-wave rectifier is exactly the same as the half-wave, but allows unidirectional current through the load during the entire sinusoidal cycle (as opposed to only half the cycle in the half-wave). A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output.



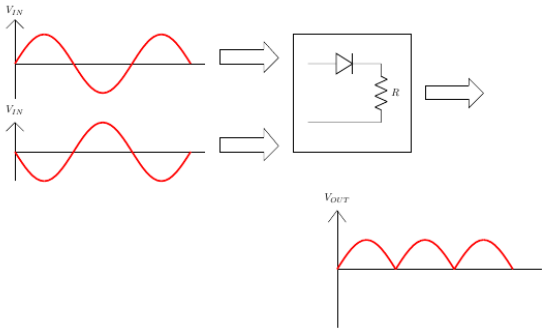
For a half wave Rectifier this is what we have observed



If we change the phase of the input waveform by 180 degrees

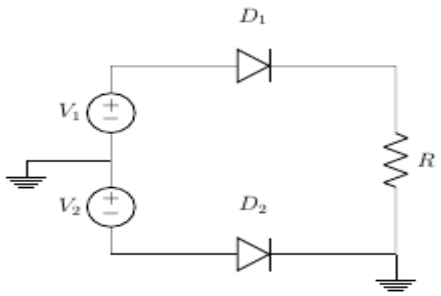


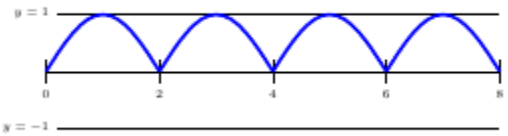
Now if we add these two circuits, we would get



Full Wave Rectifier – Circuit

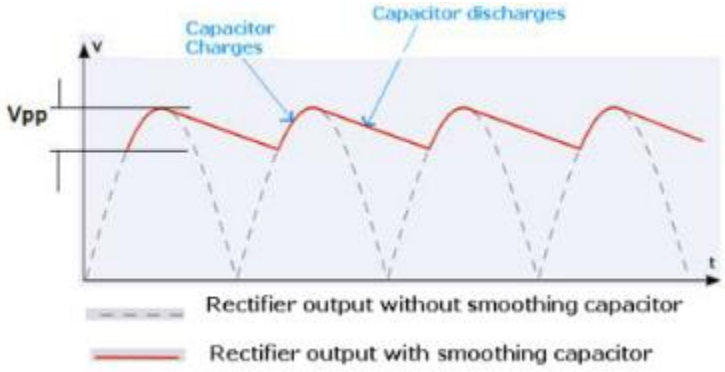
So, we have seen that this rectifier circuit consists of two sources which have a phase difference along with two diodes. When V1 is positive, V2 is negative. Hence the top diode(D1) will be a short and the bottom diode(D2) will be an open. On the other hand, when V1 is negative, V2 is positive. Hence the bottom diode(D2) will be on and the top diode(D1) will be an open circuit.





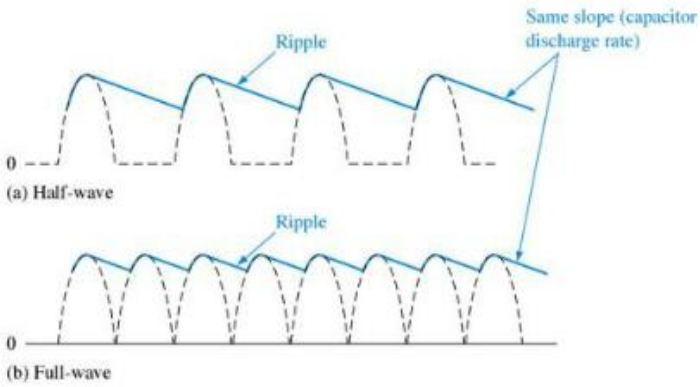
Ripple Voltage and Ripple Factor

Assuming a finite capacitor is connected, since a new charging pulse occurs every half cycle the capacitor charges and discharges very frequently. We can observe that smaller the Vpp, the more the waveform will resemble a pure DC voltage. The variable portion is known as 'ripple' and the value Vpp is known as the ripple voltage. Further the ratio of the ripple voltage to the DC or average voltage is known as the ripple factor.

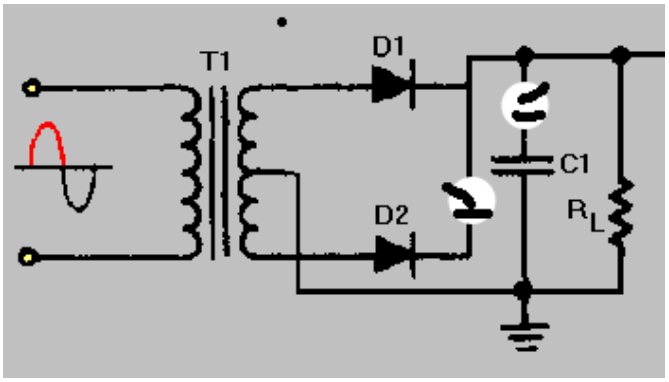


Half Wave vs Full Wave Capacitive Rectification

If the capacitance and voltage sources used are the same, which one among the two – half wave or full wave gives lesser ripple effectThe advantage of a full-wave rectifier over a half-wave is quite clear. The capacitor can more effectively reduce the ripple when the time between peaks is shorter.



Combine circuit of Full Wave and Half wave

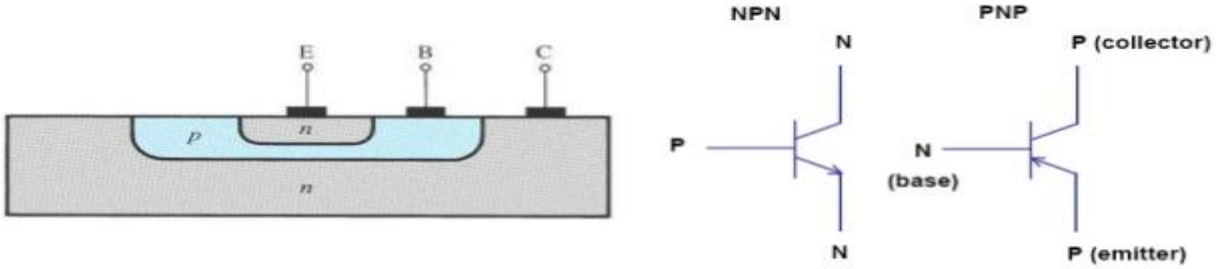


OBSERVATION TABLE:

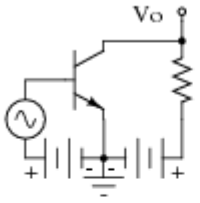
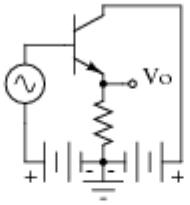
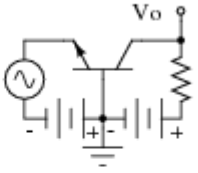
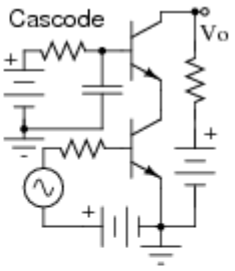
Sl no.	$V_{rms(Volt)}$	$V_{DC(Volt)}$	Ripple factor

IDENTIFICATION OF BJT (PIN)

BJT Modes



characteristics of Bipolar junction transistor in various mode

Basic circuit	Common emitter	Common collector	Common base	Cascode
				
Voltage gain	high	less than unity	high, same as CE	high, same as CB
Current gain	high	high	less than unity	high, same as CE
Power gain	high	moderate	moderate	highest
Phase inversion	yes	no	no	yes
Input impedance	moderate ≃ 1 k	highest ≃ 300 k	low ≃ 50 Ω	same as CE, ≃ 1 k
Output impedance	moderate ≃ 50 k	low ≃ 300 Ω	highest ≃ 1 Meg	same as CB, ≃ 1 Meg

Experiment-4

AIM: To study the VI charecteistics of Bipolar junction transistor in CE mode and calculate the following:

1. *Voltage gain*
2. *Current gain*
3. *Input impedance*
4. *Output impedance*

Component used:

1.BC107

2.Bread Board

3.Connecting wire

4.DMM

5. Resistor

Theory

The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification. Resistors R_{B1} and R_{B2} form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region. In order to operate transistor as an amplifier, biasing is done in such a way that the operating point is in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design V_{CE} is always set to $V_{CC}/2$. This will confirm that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. For the maximum input signal, output is produced without any distortion and clipping.

Circuit diagram

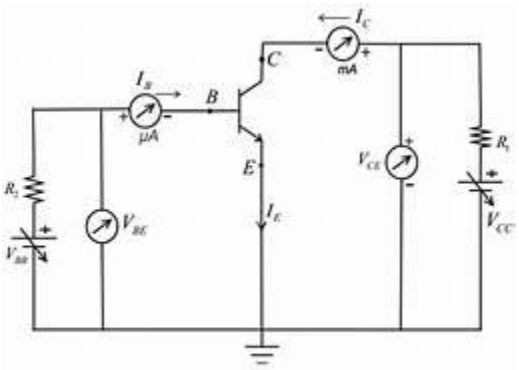
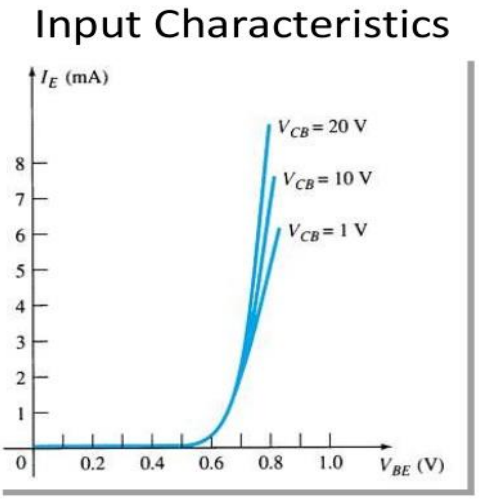
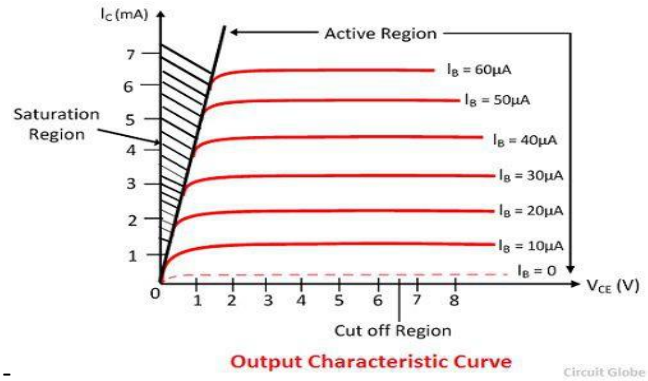


Figure 3- Circuit arrangement for studying input and output characteristics of npn transistor in CE configuration





OBSERVATION TABLE: Input characteristic

S.No	V_{CE}=1V		V_{CE}=2V	
	I_B (μA)	I_C (mA)	I_B (μA)	I_C (mA)

OBSERVATION TABLE: Output characteristic

Sl no.	*I_B=10μA*		*I_B=20μA*	
	V_{CE} (volt)	*I_C (mA)*	V_{CE} (volt)	I_C (mA)

BASIC ELECTRONICS LAB MANUAL

B.Tech (ECE)

COURSE CODE: EC291

DEPARTMENT OF ELECTRONICS & COMMUNICATION

Introduction

There are 3 periods allocated to a laboratory session in Digital Electronics. It is a necessary part of the course at which attendance is compulsory.

Here are some guidelines to help you perform the experiments and to submit the reports:

1. *Read all instructions carefully and carry them all out.*
2. *Ask a demonstrator if you are unsure of anything.*
3. *Record actual results (comment on them if they are unexpected!)*
4. *Write up full and suitable conclusions for each experiment.*
5. *If you have any doubt about the safety of any procedure, contact the demonstrator beforehand.*
6. *THINK about what you are doing!*

SYLLABUS

Basic Electronics Engineering Laboratory-I I

There will be a couple of familiarization lectures before the practical classes are undertaken where basic concept of the instruments handled will be given.

3 hours per week must be kept, initially for practical lectures, and later for tutorials.

List of Experiments:

1.Study of I-V characteristics of Field Effect Transistors.

2.Determination of input-offset voltage, input bias current and Slew rate of OPAMPs.

3.Determination of Common-mode Rejection ratio, Bandwidth and Off-set null of OPAMPs.

4.Study of OPAMP circuits: Inverting and Non-inverting amplifiers, Adders, Integrators and Differentiators.

5.Study of Logic Gates and realization of Boolean functions using Logic Gates.

6.Study of Characteristic curves for CB, CE and CC mode transistors

Experiment-1

AIM: To study the VI charecteistics of Bipolar junction transistor in CE mode and calculate the following:

1. *Voltage gain*
2. *Current gain*
3. *Input impedance*
4. *Output impedance*

Component used:

1.BC107

2.Bread Board

3.Connecting wire

4.DMM

5. Resistor

6. Power supply

Theory

The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification. Resistors R_{B1} and R_{B2} form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region. In order to operate transistor as an amplifier, biasing is done in such a way that the operating point is in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design V_{CE} is always set to $V_{CC}/2$. This will confirm that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. For the maximum input signal, output is produced without any distortion and clipping.

Circuit diagram

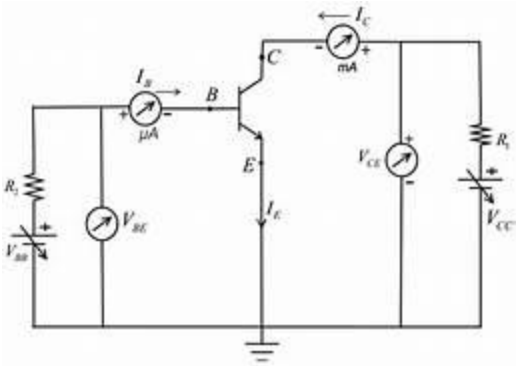
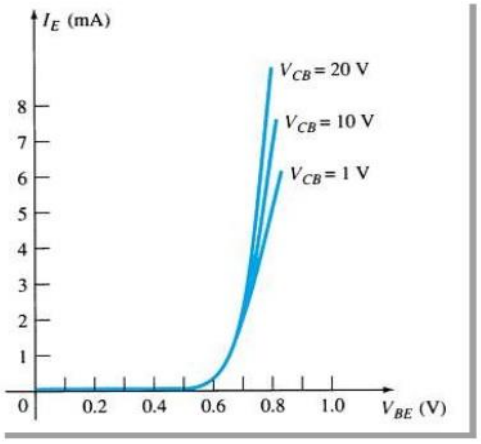
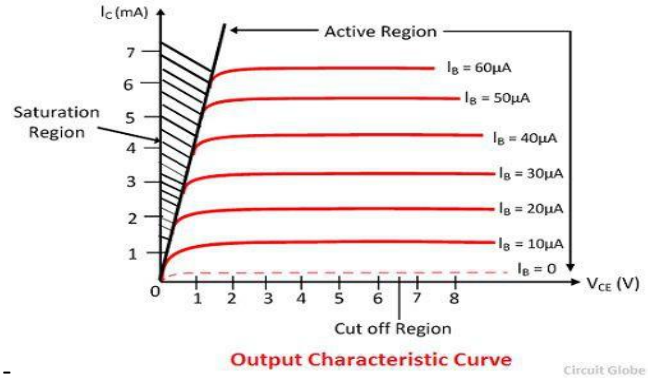


Figure 3- Circuit arrangement for studying input and output characteristics of npn transistor in CE configuration

Input Characteristics





Output Characteristic Curve

Circuit Globe

-

OBSERVATION TABLE: Input characteristic

S.No	V_{CE}=1V		V_{CE}=2V	
	I_B (μA)	I_C (mA)	I_B (μA)	I_C (mA)

OBSERVATION TABLE: Output characteristic

Sl no.	*I_B=10μA*		*I_B=20μA*	
	V_{CE} (volt)	*I_C (mA)*	V_{CE} (volt)	I_C (mA)

Experiment-2

AIM: To study the VI characteristics of Field effect transistor in n-channel mode and calculate the following:

1. *Drain resistance(r_d)*
2. *Amplification factor(μ)*
3. *Transconductance (g_m)*

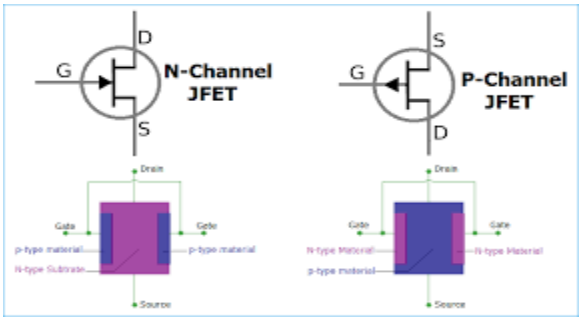
Component used:

1.BFW10
2.Bread Board
3.Connecting wire
4.DMM
5. Resistor
6. Power supply

THEORY

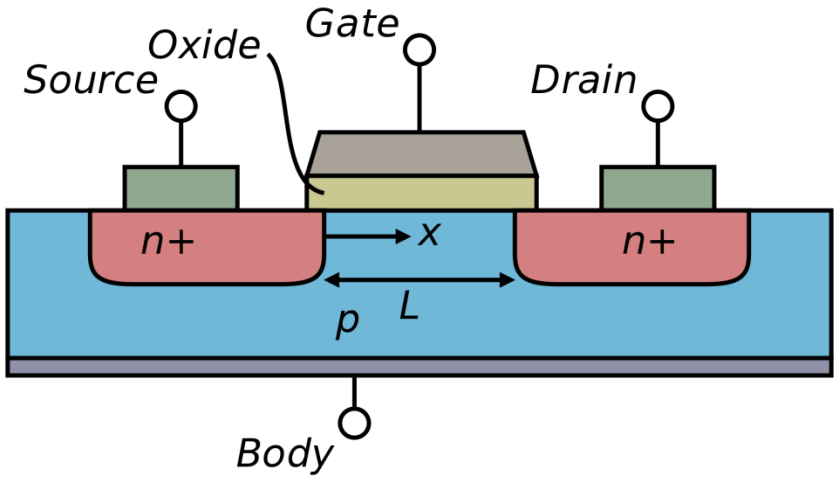
The field-effect transistor (FET) is a type of transistor that uses an electric field to control the flow of current. FETs are devices with three terminals: source, gate, and drain. FETs control the flow of current by the application of a voltage to the gate, which in turn alters the conductivity between the drain and source.

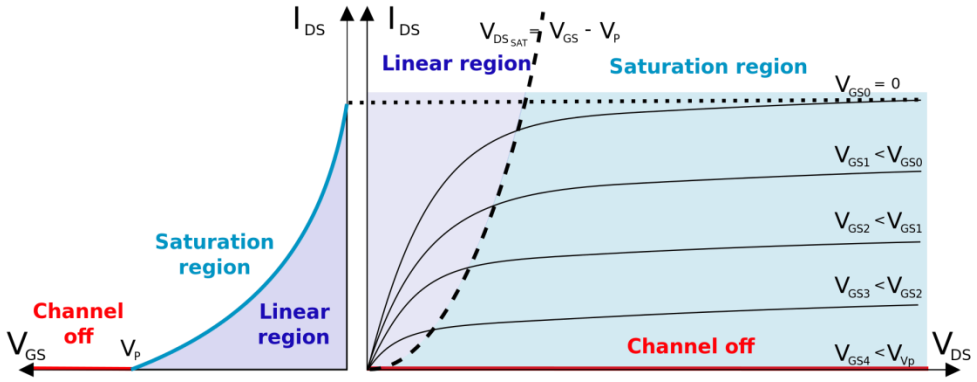
In an n-channel "depletion-mode" device, a negative gate-to-source voltage causes a depletion region to expand in width and encroach on the channel from the sides, narrowing the channel. If the active region expands to completely close the channel, the resistance of the channel from source to drain becomes large, and the FET is effectively turned off like a switch (see right figure, when there is very small current). This is called "pinch-off", and the voltage at which it occurs is called the "pinch-off voltage". Conversely, a positive gate-to-source voltage increases the channel size and allows electrons to flow easily (see right figure, when there is a conduction channel and current is large).

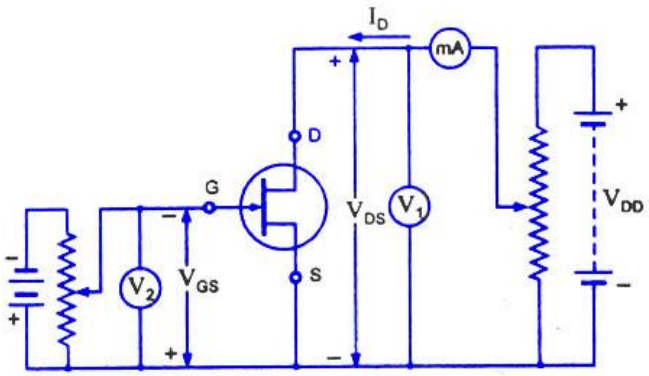


In an n-channel "enhancement-mode" device, a conductive channel does not exist naturally within the transistor, and a positive gate-to-source voltage is necessary to create one. The

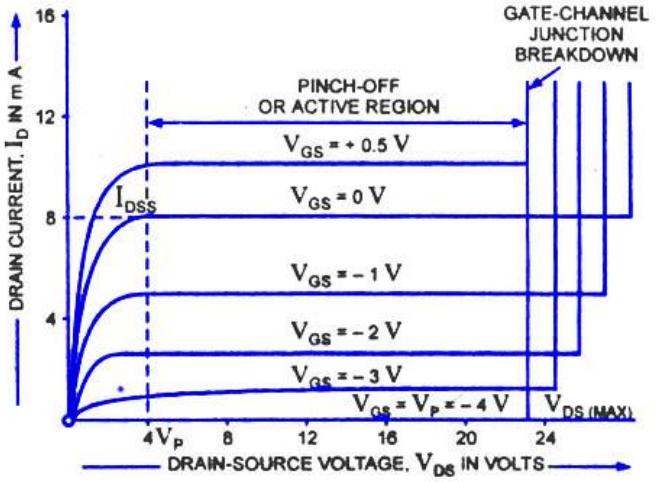
positive voltage attracts free-floating electrons within the body towards the gate, forming a conductive channel. But first, enough electrons must be attracted near the gate to counter the dopant ions added to the body of the FET; this forms a region with no mobile carriers called a depletion region, and the voltage at which this occurs is referred to as the threshold voltage of the FET. Further gate-to-source voltage increase will attract even more electrons towards the gate which are able to create a conductive channel from source to drain; this process is called inversion.







Circuit Diagram For Determining Drain Characteristic With External Bias For An N-Channel JFET



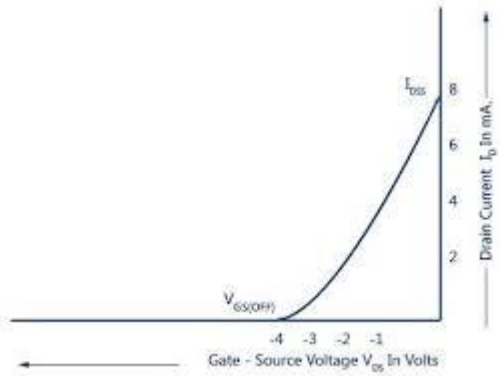
JFET Drain-Characteristics With External Bias

Drain Characteristic

SL no.	V_{GS}= 1V		V_{GS} = *2V*	
	V_{DS} *(V)*	I_D *(mA)*	V_{DS} *(V)*	I_D *(mA)*

Transfer characteristics

Sl no.	V_{DS}= *(V)*	
	V_{GS} *(V)*	$I_{D(}$ (mA)



Experiment-3

Experiment Name: Realization of Basic gates using universal logic gates.

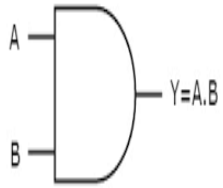
components used:

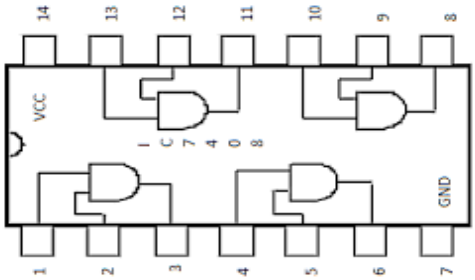
1. Digital I.C Trainer Kit.
2. Single strand wire.
3. Cutter.
4. Tweezers.
5. I.C.—i) 7408 –AND ii) 7432-OR, iii) 7404-NOT ,iv) v) 7400- NAND v) 7402- NOR

THEORY: ***BASIC GATES-*** *i) AND, ii) OR, iii) NOT*

AND gate- The AND gate is a basic digital logic gate that implements logical conjunction - it behaves according to the truth table to the right. A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If none or not all inputs to the AND gate are HIGH, LOW output results.

Truth Table

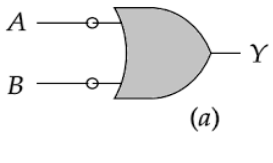


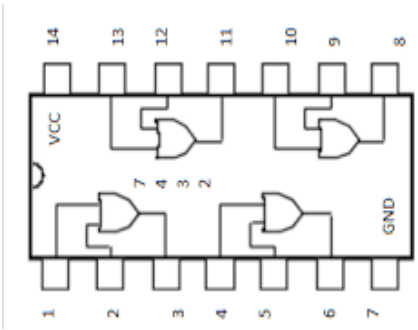


Input		O/P
X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

OR gate- *The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB*

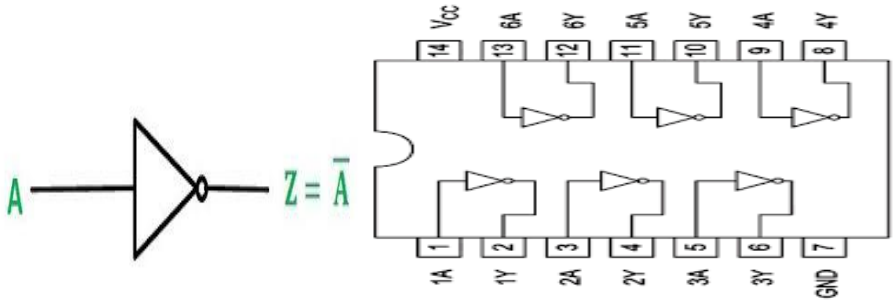
Truth Table





Input		O/P
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

NOT gate- *The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs. The diagrams below show two ways that the NAND logic gate can be configured to produce a NOT gate. It can also be done using NOR logic gates in the same way.*

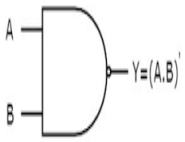


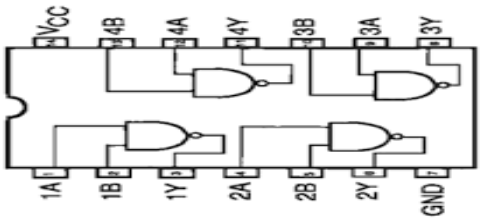
Input	Output
X	Y
0	1
1	0

UNIVERSAL GATES- *i) NAND ii) NOR*

NAND gate- This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion

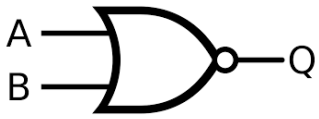
Truth Table

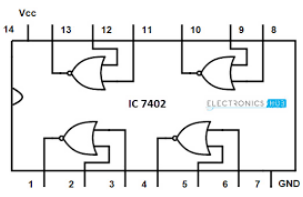




Input		O/P
X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

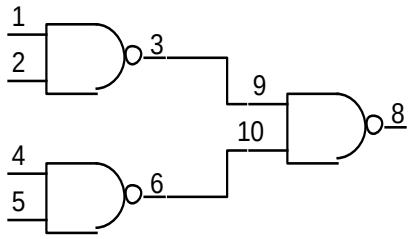
NOR gate- *This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high.*
The symbol is an OR gate with a small circle on the output. The small circle represents inversion.



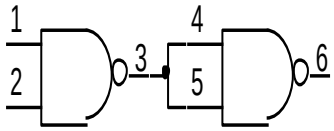


Input		O/P
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

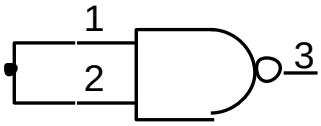
CIRCUIT*:* ***Basic gates using NAND gates***



OR gate using NAND gate

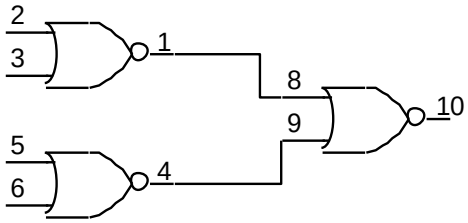


AND gate using NAND gate

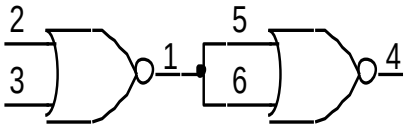


NOT gate using NAND gate

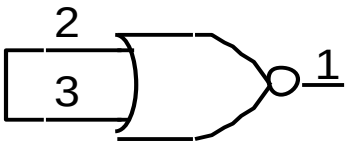
Basic gates using NOR gates



AND gate using NOR gate



OR gate using NOR gate



NOT gate using NOR gate

Experiment-4

AIM: To study and calculate the gain of different types of op-amp. They are

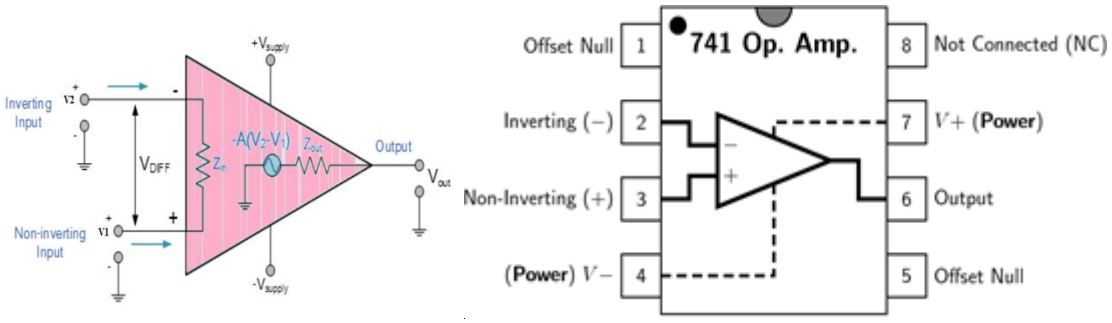
1. *INVERTING AMPLIFIER*
2. *NON- INVERTING AMPLIFIER*
3. *SUMMING AMPLIFIER*
4. *INTEGRATING AMPLIFIER*
5. *DIFFERENTIATOR*

components used:

1. *Op -amp Ic-741*
2. *Bread board*
3. *Resistor*
4. *Capacitor*
5. *Connecting wires*

THEORY

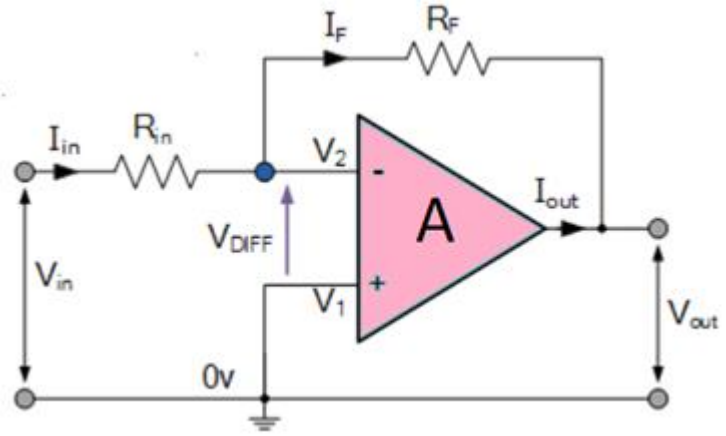
Operational Amplifier commonly known as Op-Amp, is a linear electronic device having three terminals, two high impedance input and one output terminal. Op-Amp can perform multiple function when attached to different feedback combinations like resistive, capacitive or both. Generally it is used as voltage amplifier and the output voltage of the Op-Amp is the difference between the voltages at its two input terminals.



Op-Amp shows some properties that make it an ideal amplifier, its open loop gain and input impedance is infinite (i.e. Practically very high), Output impedance and offset voltage is zero(i.e. Practically very low) and bandwidth is infinite(i.e. Practically limited to frequency where its gain become unity).

Inverting Op-Amp:

The open loop gain(Ao) of the Om-Amp is very high which makes it very unstable, so to make it stable with a controllable gain, a feed back is applied through some external resistor(Fry) from its output to inverting input terminal(i.e. Also known as negative feedback) resulting in reduced gain(closed loop gain, Av). So the voltage at inverting terminal is now the sum of the actual input and feedback voltages, and to separate both a input resistor(RI) is introduced in the circuit. The non inverting terminal of the pomp is grounded, and the inverting terminal behaves like a virtual ground as the junction of the input and feedback signal are at the same potential.



The close loop gain (A_{cl}) is given by :-_ $A_{cl}=V_{out}tV_{in}=-R_F/R_{in}$

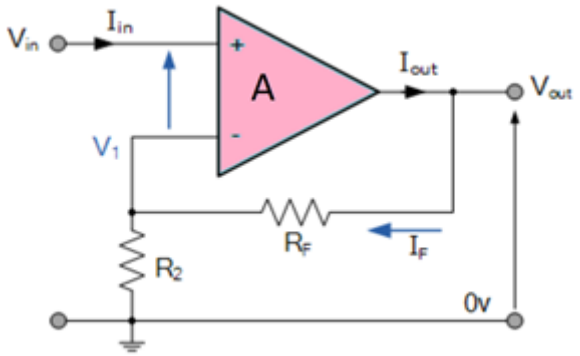
Output voltage (V_{out}) is given by :- $V_{out}=-R_F/R_{in}\times V_{in}$

OBSERVATION TABLE:

Sl no.	*V_{in}(volt)*	*$A_V=-R_F/R_{in}$*	*V_{out} (volt)*

Non-Inverting Op-Amp

In this configuration of Op-amp the input signal is directly fed to the non inverting terminal resulting in a positive gain and output voltage in phase with input as compared to inverting Op-amp where the gain is negative and output voltage is out of phase with input , and to stabalize the circuit a negative feedback is applied through a resistor(Rf) and the inverting terminal is grounded with input resistor(R2).This inverting Op-Amp like layout the at inverting terminal creates a virtual ground at the summing point make the Rf and R2 a potential divider across inverting terminal, Hence determines the gain of the circuit.



Output Voltage (Vout) is given by:

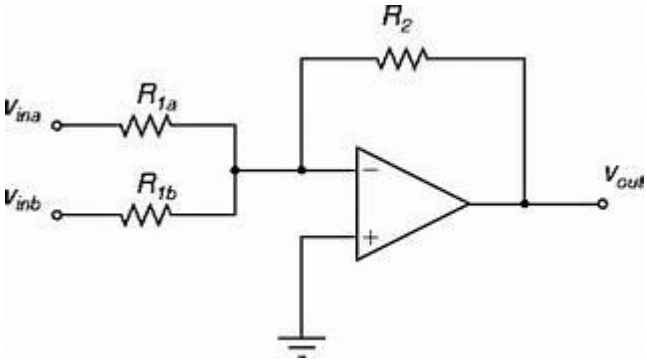
OBSERVATION TABLE:

Sl no.	*V_{in}(volt)*	*$A_V=1+R_F/R_{in}$*	*V_{out} (volt)*

Summing amplifier

Summing amplifier is basically an op amp circuit that can combine numbers of input signal to a single output that is the weighted sum of the applied inputs. The summing Amplifier is one variation of inverting amplifier. In inverting amplifier there is only one voltage signal applied to the inverting input as shown below,

Summing Amplifier or Op Amp Adder Circuit Diagram

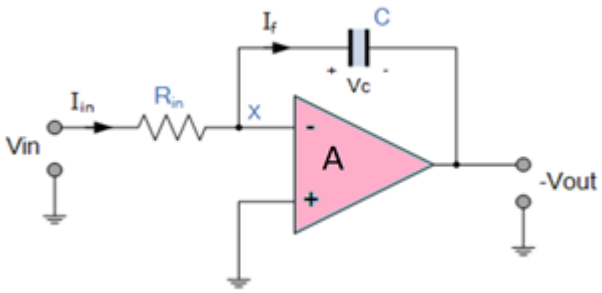


OBSERVATION TABLE:

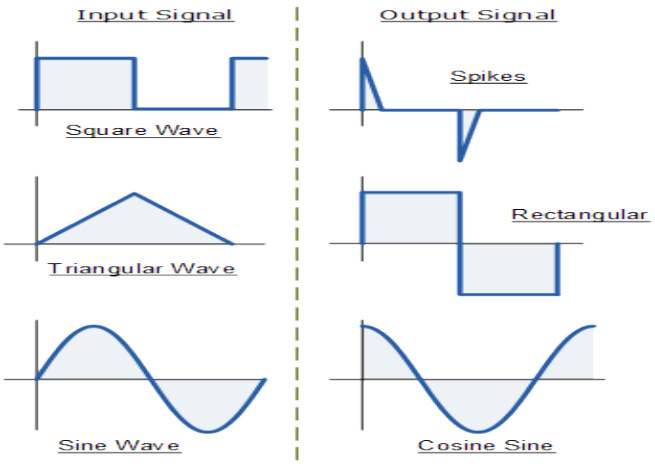
Sl no.	*V_{in}(volt)*	*V_{out} (volt)*

The Integrator

It is a circuit designed with Op-Amp in such a way that it performs the mathematical Integration operation, its output is proportional to the amplitude and time duration of the input applied. The integrator circuit layout is same as a inverting amplifier but the feedback resistor is replaced by a capacitor which make the circuit frequency dependent. In this case the circuit is derived by the time duration of input applied which results in the charging and discharging of the capacitor. Initially when the voltage is applied to integrator the uncharged capacitor allows maximum current to pass through it and no current flows through the Op-Amp due to the presence of virtual ground, the capacitor starts to charge at the rate of RC time constant and its impedance starts to increase with time and a potential difference is develops across the capacitor resulting in charging current to decrease. This results in the ratio of capacitor's impedance and input resistance increasing causing a linearly increasing ramp output voltage that continues to increase until the capacitor becomes fully charged.

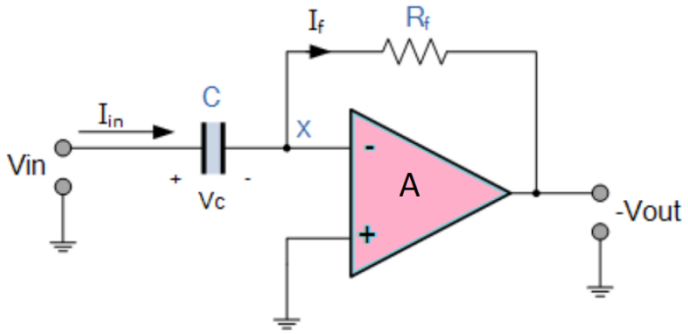


Wave forms-

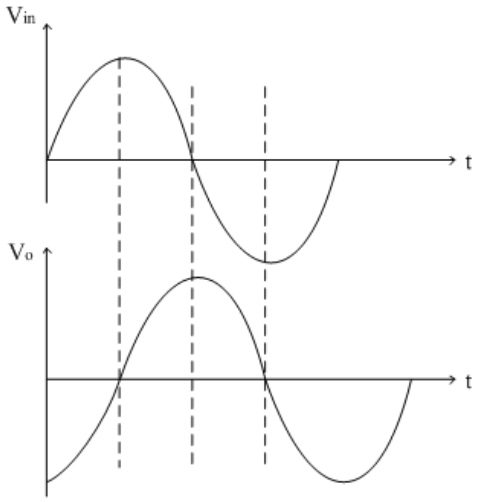


The Differentiator

*In the differentiator circuit the input is connected to the inverting output of the Op-Amp through a capacitor(C) and a negetive feedback is provided to the inverting input terminal through a resistor(Rf), which is same as an integrator circuit with feedback capacitor and input resistor being replaced with each other. Here the circuit performs a mathematical differentiation operation, and the output is the first derivative of the input signal, 180' out of phase and amplified with a factor Rf*C. The capacitor on the input allows only the AC component and restrict the DC, at low frequency the reactance of capacitor is very high causing a low gain and high frequency vice versa but and high frequency the circuit becomes unstable.*



Wave forms



SILIGURI INSTITUTE OF TECHNOLOGY

LAB MANUAL

DIGITAL SYSTEM DESIGN LAB
(EC-392)

3RD SEM (ECE)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG
SILIGURI INSTITUTE OF TECHNOLOGY

CONTENTS

SUBECT: DIGITAL SYSTEM DESIGN LAB (EC392)

EXPERIMENT NO: 1

Aim: - Introduction to Digital Electronics Lab- Nomenclature of Digital Ics, Specifications, Study of the Data Sheet, Concept of V_{cc} and Ground, Verification of the Truth Tables of Logic Gates using TTL Ics.

APPARATUS REQUIRED: Power Supply, Digital Trainer Kit., Connecting Leads, IC's (7400, 7402, 7404, 7408, 7432, and 7486)

BRIEF THEORY:

AND Gate: The AND operation is defined as the output as (1) one if and only if all the inputs are (1) one. 7408 is the two Inputs AND gate IC.A&B are the Input terminals &Y is the Output terminal.

$$Y = A.B$$

OR Gate: The OR operation is defined as the output as (1) one if one or more than 0 inputs are (1) one. 7432 is the two Input OR gate IC. A&B are the input terminals & Y is the Output terminal.

$$Y = A + B$$

NOT GATE: The NOT gate is also known as Inverter. It has one input (A) & one output (Y). IC No. is 7404. Its logical equation is,

$$Y = A \text{ NOT } B,\ Y = A'$$

NAND GATE: The IC no. for NAND gate is 7400. The NOT-AND operation is known as NAND operation. If all inputs are 1 then output produced is 0. NAND gate is inverted AND gate.

$$Y = (A.\ B)'$$

NOR GATE: The NOR gate has two or more input signals but only one output signal. IC 7402 is two I/P IC. The NOT- OR operation is known as NOR operation. If all the inputs are 0 then the O/P is 1. NOR gate is inverted OR gate.

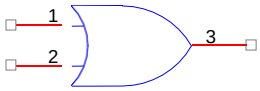
$$Y = (A+B)'$$

EX-OR GATE: The EX-OR gate can have two or more inputs but produce one output. 7486 is two inputs IC. EX-OR gate is not a basic operation & can be performed using basic gates.

$$Y = A \dotplus B$$

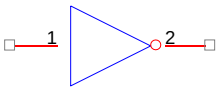
LOGIC SYMBOL:

. Logic Symbol of Gates



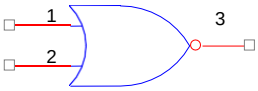
OR

AND

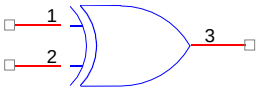


NOT

NAND



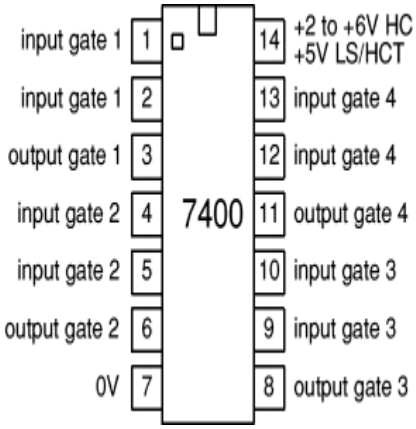
NOR



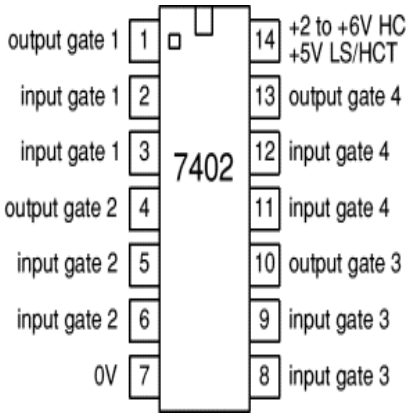
XOR

PIN CONFIGURATION:

7400(NAND)

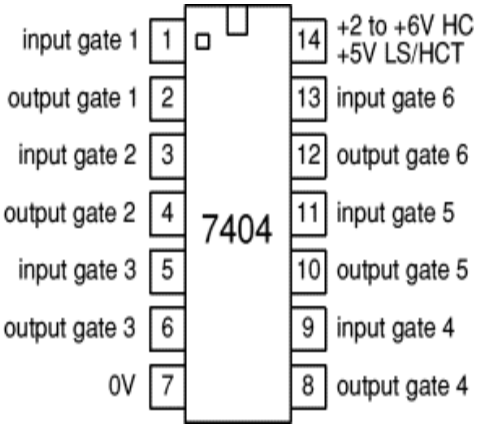


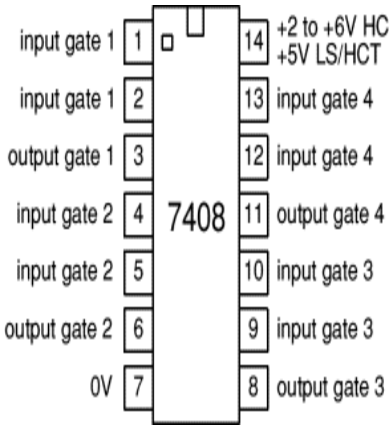
7402(NOR)



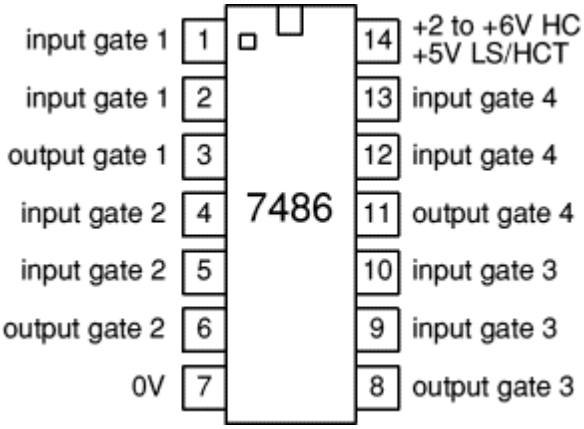
7404(NOT)

7408 (AND)

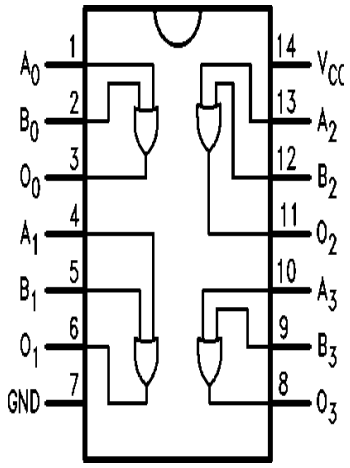




7486(EX-OR)



7432(OR)



PROCEDURE:

(a) Fix the IC's on breadboard & give the supply.
(b) Connect the +ve terminal of supply to pin 14 & -ve to pin 7.
(c) Give input at pin 1, 2 & take output from pin 3. It is same for all except NOT & NOR IC.
(d) For NOR, pin 1 is output & pin 2&3 are inputs.
(e) For NOT, pin 1 is input & pin 2 is output.
(f) Note the values of output for different combination of inputs & draw the TRUTH TABLE.

OBSERVATION TABLE:

INPUTS		**OUTPUTS**					
A	**B**	**A'**	**A+B**	**(A+B)'**	**(A*B)**	**(A*B)'**	**(A⊕B)**

		NOT	OR	NOR	AND	NAND	Ex-OR
0	**0**	**1**	**0**	**1**	**0**	**1**	**0**
0	**1**	**1**	**1**	**0**	**0**	**1**	**1**
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**
1	**1**	**0**	**1**	**0**	**1**	**0**	**0**

RESULT: We have learnt all the gates ICs according to the IC pin diagram.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Define gates ?

Ans. Gates are the digital circuits, which perform a specific type of logical operation.

Define IC?

Ans. IC means integrated circuit. It is the integration of no. of components on a common substrate.

Give example of Demorgan's theorem.

Ans. (AB)'=A'+B'

(A+B)'=A'.B'

(A+A) A =?

Ans. A.

Q5 Define Universal gates.

Ans. Universal gates are those gates by using which we can design any type of logical expression.

Q6.Write the logical equation for AND gate.

Ans. Y=A.B

Q7 How many no. of input variables can a NOT Gate have?

Ans. One.

Q8.Under what conditions the output of a two input AND gate is one?

Ans. Both the inputs are one.

Q9.1+0 =?

Ans. 1

Q10.When will the output of a NAND Gate be 0?

Ans. When all the inputs are 1.

EXPERIMENT NO: 2

Aim: Implementation of the Given Boolean Function using Logic Gates in Both Sop and Pos Forms.

APPARATUS REQUIRED: Power Supply, Digital Trainer, IC's (7404, 7408, 7432) Connecting leads.

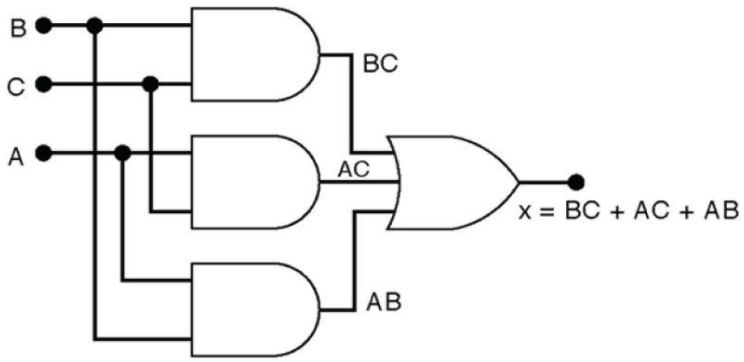
BRIEF THEORY: Karnaugh maps are the most extensively used tool for simplification of Boolean functions. It is mostly used for functions having up to six variables beyond which it becomes very cumbersome. In an n-variable K-map there are 2^n cells. Each cell corresponds to one of the combination of n variable, since there are 2^n combinations of n-variables. Gray code has been used for the identification of cells.

Example- f (A, B, C, D) =A'BC+AB'C+ABC'+ABC (SOP)

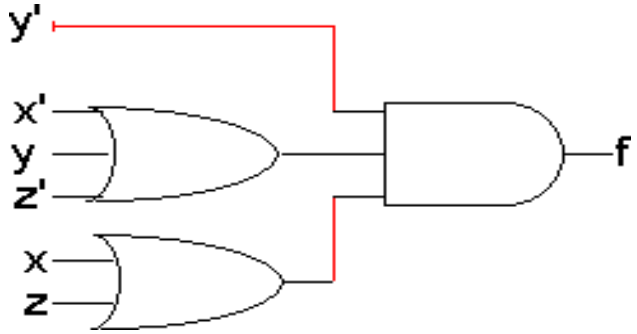
Reduced form is BC+AC+AB and POS form is f(X, Y, Z) = Y' (X'+Y+Z') (X+Z)

LOGIC DIAGRAM

SOP form



POS Form



PROCEDURE:

(a) With given equation in SOP/POS forms first of all draw a K-map.
(b) Enter the values of the O/P variable in each cell corresponding to its Min/Max term.
(c) Make group of adjacent ones.
(d) From group write the minimized equation.
(e) Design the ckt. of minimized equation & verify the truth table.

RESULT/CONCLUSION: Implementation of SOP and POS form is obtained with AND and OR gates.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Define K-map ?
Ans. It is a method of simplifying Boolean Functions in a systematic mathematical way.
Define SOP ? Ans.
Sum of Product.
Define POS ? Ans.
Product of Sum.
What are combinational circuits?
Ans. These are those circuits whose output depends upon the inputs present at that instant of time.
What are sequential circuits?
Ans. These are those circuits whose output depends upon the input present at that time as well as the previous output.
If there are four variables how many cells the K-map will have?
Ans. 16.
When two min-terms can be adjacent?
Ans. 2 to the power n.
Which code is used for the identification of cells?
Ans8. Gray Code.
Define Byte?
Ans. Byte is a combination of 8 bits.
When simplified with Boolean Algebra $(x + y)(x + z)$ simplifies toAns.
$x + yz$

EXPERIMENT NO: 3

Aim: Verification of State Tables of Rs, J-k, T and D Flip-Flops using NAND & NOR Gates

APPARATUS REQUIRED: IC' S 7400, 7402 Digital Trainer & Connecting leads.

BRIEF THEORY:

- **RS FLIP-FLOP:** There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. When I/Ps R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

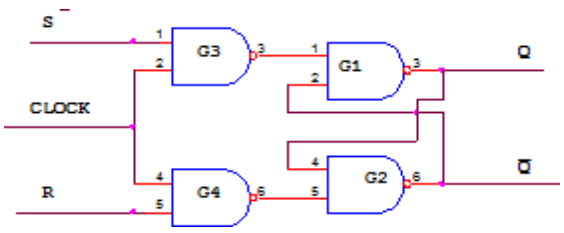
- **JK FLIP-FLOP**: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip- flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disabled and Q retains its last value.

- **D FLIP –FLOP**: This kind of flip flop prevents the value of D from reaching the Q output until clock pulses occur. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

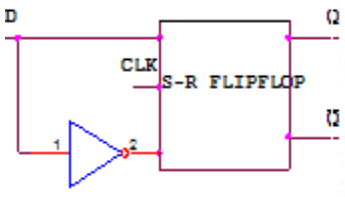
- **T FLIP-FLOP**: The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

CIRCUIT DIAGRAM:

SR Flip Flop

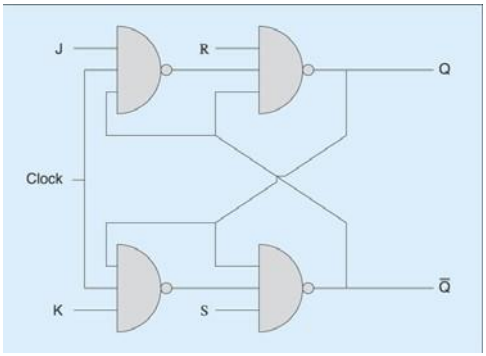


D Flip Flop



JK Flip Flop

T Flip Flop



PROCEDURE:

1. Connect the circuit as shown in figure.
2. Apply Vcc & ground signal to every IC.
3. Observe the input & output according to the truth table.

TRUTH TABLE:
SR FLIP FLOP:

CLOCK	S	R	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	?

D FLIPFLOP:

INPUT	OUTPUT
0	0
1	1

JK FLIPFLOP

CLOCK	S	R	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	Qn’

T FLIPFLOP

CLOCK	S	R	Q_{n+1}

1	**0**	**1**	**NO CHANGE**
1	**1**	**0**	**Qn'**

RESULT: Truth table is verified on digital trainer.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q 1.Flip flop is Astable or Bistable?
Ans. Bistable.
Q2.What are the I/Ps of JK flip–flop where this race round condition occurs?
Ans. Both the inputs are 1.
Q3.When RS flip-flop is said to be in a SET state?
Ans. When the output is 1.
Q4.When RS flip-flop is said to be in a RESET state?
Ans. When the output is 0.
Q5.What is the truth table of JK flip-flop?

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n,

Q6.What is the function of clock signal in flip-flop?
Ans. To get the output at known time.
Q7.What is the advantage of JK flip-flop over RS flip-flop?
Ans. In RS flip-flop when both the inputs are 1 output is undetermined.
Q8.In D flip-flop I/P = 0 what is O/P?
Ans.0
Q9.In D flip-flop I/P = 1 what is O/P?
Ans.1
Q10.In T flip-flop I/P = 1 what is O/P?
Ans. Qn

EXPERIMENT NO: 4

Aim:- Implementation and Verification of Decoder/De-Multiplexer and Encoder using Logic Gates.

APPARATUS REQUIRED: IC 7447, 7-segment display, IC 74139 and connecting leads.

BRIEF THEORY:

ENCODER: An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security, or saving space by shrinking size. An encoder has M input and N output lines. Out of M input lines only one is activated at a time and produces equivalent code on output N lines. If a device output code has fewer bits than the input code has, the device is usually called an encoder. For example Octal-to-Binary Encoder take 8 inputs and provides 3 outputs, thus doing the opposite of what the 3-to-8 decoder does. At any one time, only one input line has a value of 1. The figure below shows the truth table of an Octal-to-binary encoder.

For an 8-to-3 binary encoder with inputs I0-I7 the logic expressions of the outputs Y0-Y2 are:

$$Y0 = I1 + I3 + I5 + I7$$

$$Y1 = I2 + I3 + I6 + I7$$

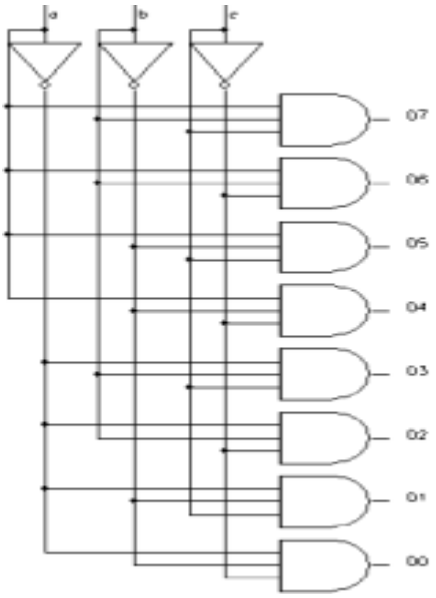
$$Y2 = I4 + I5 + I6 + I7$$

DECODER: A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2^n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. In case of decoding all combinations of three bits eight (2^3=8) decoding gates are required. This type of decoder is called 3-8 decoder because 3 inputs and 8 outputs. For any input combination decoder outputs are 1.

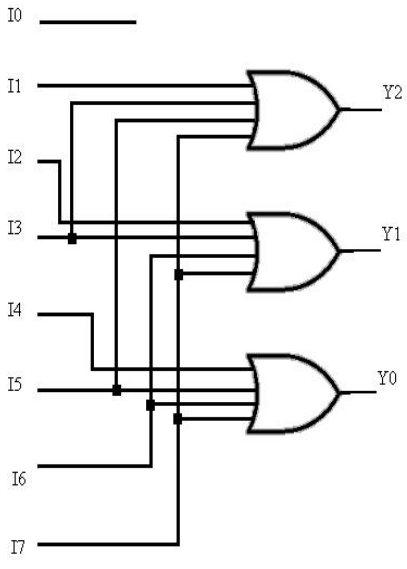
DEMULTIPLEXER: Demultiplexer means generally one into many. A demultiplexer is a logic circuit with one input and many outputs. By applying control signals, we can steer the input signal to one of the output lines. The ckt. has one input signal, m control signal and n output signals. Where 2^n = m. It functions as an electronic switch to route an incoming data signal to one of several outputs.

LOGIC DIAGRAM:

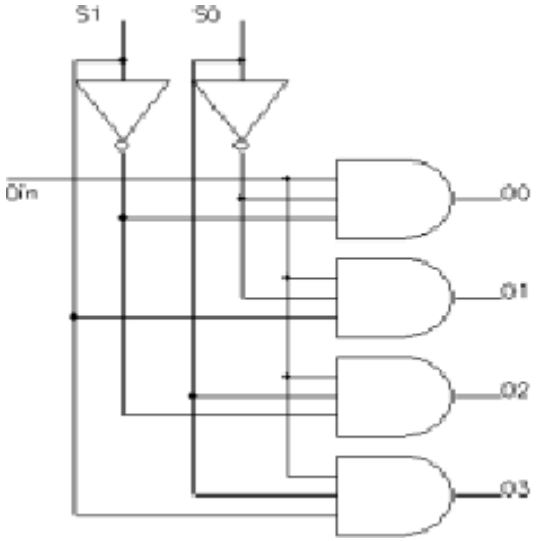
3:8 Decoder



Octal to Binary Encoder



1:4 Demux



PROCEDURE:

1) Connect the circuit as shown in figure.
2) Apply Vcc & ground signal to every IC.
3) Observe the input & output according to the truth table.

OBSERVATION TABLE:

Truth table for Decoder

Inputs			Outputs							
a	b	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1
Output function			$\bar{a}\bar{b}\bar{c}$	$\bar{a}\bar{b}c$	$\bar{a}b\bar{c}$	$\bar{a}bc$	$a\bar{b}\bar{c}$	$a\bar{b}c$	$ab\bar{c}$	abc

Truth table for Encoder

I0	I1	I2	I3	I4	I5	I6	I7	Y2	Y1	Y0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Truth table for Demux

Output select Lines		Output selected
S_1	S_0	
0	0	O_0
0	1	O_1
1	0	O_2
1	1	O_3

RESULT: Encoder/ decoder and demultiplexer have been studied and verified.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q. 1 What do you understand by decoder?
Ans. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines. Most IC decoders include one or more enable inputs to control the circuit operation.
Q. 2 What is demultiplexer?

Ans. The demultiplexer is the inverse of the multiplexer, in that it takes a single data input and n address inputs. It has 2^n outputs. The address input determine which data output is going to have the same value as the data input. The other data outputs will have the value 0.

Q. 3 What do you understand by encoder?

Ans. An encoder or multiplexer is therefore a digital IC that outputs a digital code based on which of its several digital inputs is enabled.

Q. 4 What is the main difference between decoder and demultiplexer?

Ans. In decoder we have n input lines as in demultiplexer we have n select lines.

Q. 5 Why Binary is different from Gray code?

Ans. Gray code has a unique property that any two adjacent gray codes differ by only a single bit.

Q. 6 Write down the method of Binary to Gray conversion.

Ans. Using the Ex-Or gates.

Q. 7 Convert 0101 to Decimal**.**

Ans. 5

Q. 8 Write the full form of ASCII Codes?

Ans. American Standard Code for Information Interchange.

Q.9. If a register containing 0.110011 is logically added to register containing 0.101010 what would be the result?

Ans.111011

Q10.Binary code is a weighted code or not?

Ans. Yes

EXPERIMENT NO : 5

Aim: Implementation of 4x1 Multiplexer using Logic Gates.

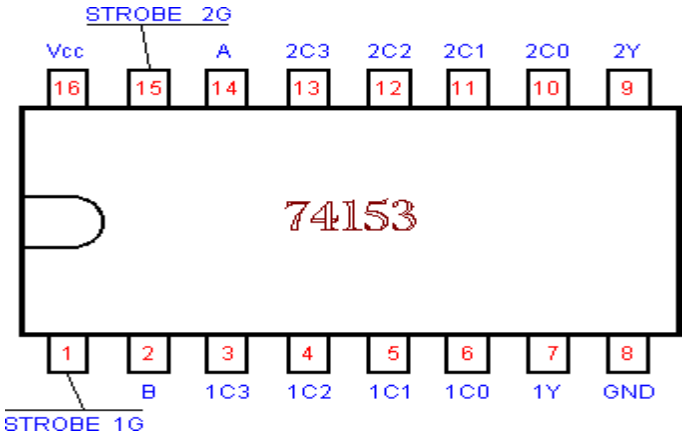
APPARATUS REQUIRED: Power Supply, Digital Trainer, Connecting Leads, IC's 74153(4x1 multiplexer).

BRIEF THEORY:

MULTIPLEXER: Multiplexer generally means many into one. A multiplexer is a circuit with many Inputs but only one output. By applying control signals we can steer any input to the output .The fig. (1) Shows the general idea. The ckt. has n-input signal, control signal & one output signal. Where $2^n = m$. One of the popular multiplexer is the 16 to 1 multiplexer, which has 16 input bits, 4 control bits & 1 output bit.

PIN CONFIGURATION;–

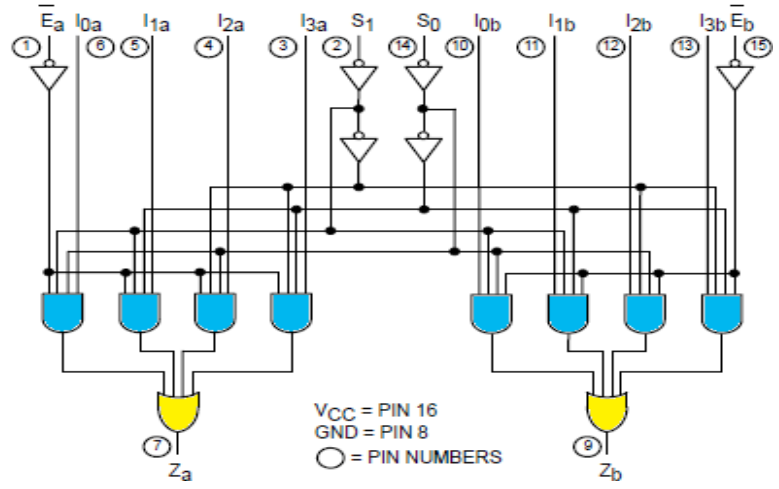
IC 74153 (4x1 multiplexer)



LOGIC DIAGRAM:

Multiplexer (4x1) IC 74153

LOGIC DIAGRAM



PROCEDURE:

1. Fix the IC's on the bread board &give the input supply.
2. Make connection according to the circuit.
3. Give select signal and strobe signal at respective pins.
4. Connect +5 v Vcc supply at pin no 24 & GND at pin no 12.
5. Verify the truth table for various inputs.

OBSERVATION TABLE:

Truth Table of multiplexer (4x1) IC 74153

INPUT							OUTPUT
A	B	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

RESULT: Verify the truth table of multiplexer for various inputs.
PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Why is MUX called as "Data Selector"?
Ans. This selects one out of many inputs.
What do you mean by Multiplexing?
Ans. Multiplexing means selecting only a single input out of many inputs.
What is Digital Multiplexer?
Ans. The multiplexer which acts on digital data.
What is the function of Enable input to any IC?
Ans. When this enable signal is activated.
What is demultiplexer?
Ans. A demultiplexer transmits the data from a single source to various sources.
Can a decoder function as a D'MUX?
Ans. Yes
What is the role of select lines in a Demultiplexer?
Ans. Select line selects the output line.
Differentiate between functions of MUX & D'MUX?
Ans. Multiplexer has only single output but demultiplexer has many outputs.
The number of control lines required for a 1:8 demultiplexer will be
Ans. 3
How many 4:1 multiplexers will be required to design 8:1 multiplexer?Ans.
2

EXPERIMENT NO - 6

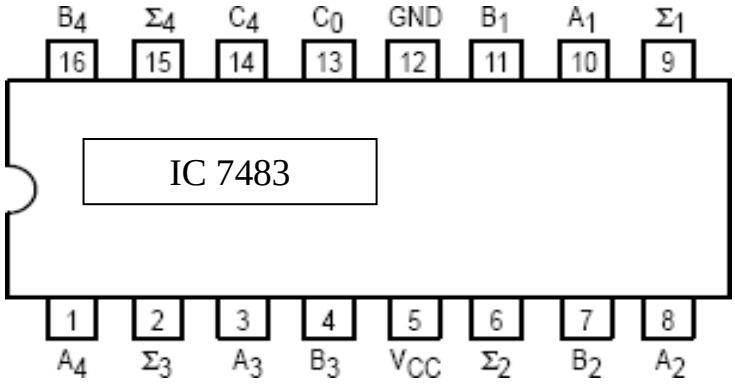
Aim – Implementation of 4-Bit Parallel Adder Using 7483 Ic.

APPRATUS REQUIRED – Digital trainer kit, IC 7483 (4-bit parallel adder).

BRIEF THEOR - A 4-bit adder is a circuit which adds two 4-bits numbers, say, A and B. In addition, a 4-bit adder will have another single-bit input which is added to the two numbers called the carry-in (C_{in}). The output of the 4-bit adder is a 4-bit sum (S) and a carry-out (C_{out}) bit.

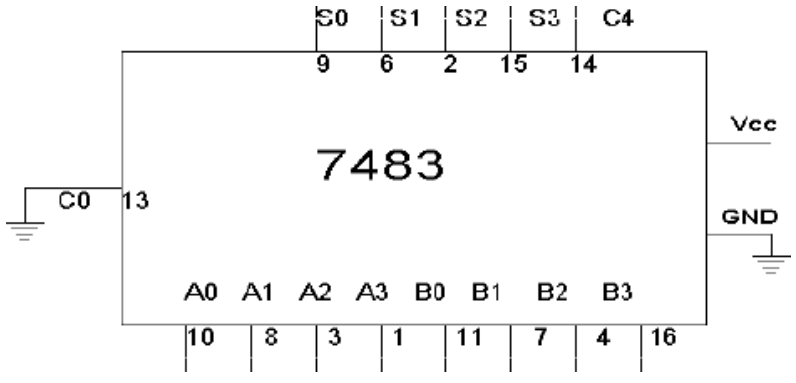
PIN CONFIGURATION–

Pin Diagram of IC 7483



LOGIC DIAGRAM:-

7483 4-bit Parallel Adder



OBSERVATION TABLE –

Truth table of 4-bit parallel adder

A3	A2	A1	A0	B3	B2	B1	B0	C4 (V)	S3(V)	S2(V)	S1(V)	S0(V)
0	0	0	1	0	0	1	0	0	0	0	1	1
0	1	0	1	1	0	1	1	1	1	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	0	0	1	1	0	1	0	1	0

PROCEDURE –

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT- Binary 4-bit full adder is studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q 1 What do you understand by parallel adder?
Ans. If we place full adders in parallel, we can add two- or four-digit numbers or any other size desired i.e. known as parallel adder.
Q2 What happens when an *N*-bit adder adds two numbers whose sum is greater than or equal to 2^N
Ans. Overflow.
Q3 Is Excess-3 code is weighted code or not?
Ans. Excess-3 is not a weighted code.
Q4 What is IC no. of parallel adder?
Ans. IC 7483.
Q5 What is the difference between Excess-3 & Natural BCD code?
Ans. Natural BCD code is weighted code but Excess-3 code is not weighted code.
Q6. What is the Excess-3 code for $(396)_{10}$
Ans. $(396)_{10} = (011011001001)_{EX-3}$
Q7 Can we obtain 1's complement using parallel adder?
Ans. Yes
Q8 Can we obtain 2's complement using parallel adder?
Ans. yes
Q9 How many bits can be added using IC7483 parallel adder?

Ans. 4 bits.
Q10 Can you obtain subtractor using parallel adder?
Ans. Yes

EXPERIMENT NO :7

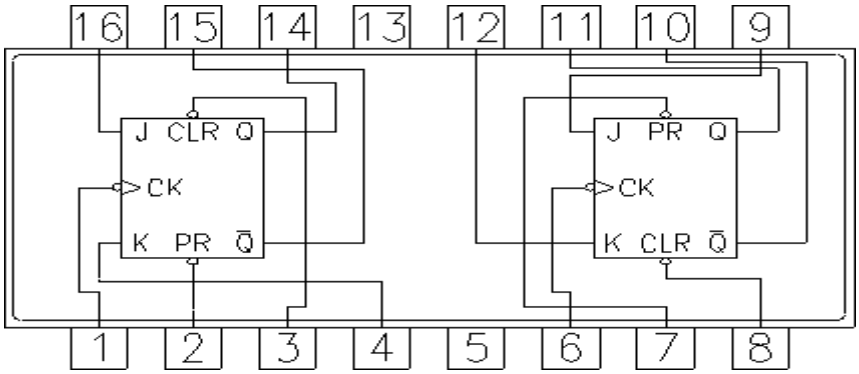
Aim: – Design, and Verify the 4-Bit Synchronous Counter

APPARATUS REQUIRED: Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

BRIEF THEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

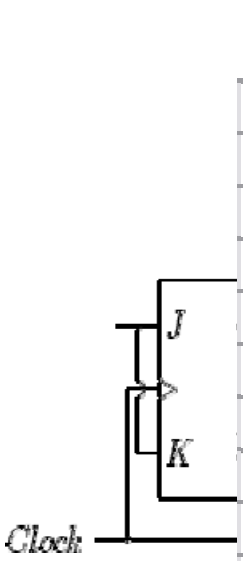
PIN CONFIGURATION:

Dual JK Master Slave Flip Flop with clear & preset



LOGIC DIAGRAM:

4-Bit Synchronous counter



Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

OBSERVATION TABLE:

Truth Table

States				Count
0_4	0_3	0_2	0_1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT: 4-bit synchronous counter studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 What do you understand by counter?
Ans. Counter is a register which counts the sequence in binary form.
Q.2What is asynchronous counter?
Ans. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.
Q.3What is synchronous counter?
Ans. Where Clock input is common to all FF.
Q.4Which flip flop is used in asynchronous counter?
Ans. All Flip-Flops are toggling FF.
Q.5Which flip flop is used in synchronous counter?
Ans. Any FF can be used.
What do you understand by modulus?
Ans. The total no. of states in counter is called as modulus. If counter is modulus-n, then it has n different states.
What do you understand by state diagram?
Ans. State diagram of counter is a pictorial representation of counter states directed by arrows in graph.
What do you understand by up/down counter?
Ans. Up/Down Synchronous Counter: two way counter which able to count up or down.
Why Asynchronous counter is known as ripple counter?
Ans. Asynchronous Counter: flip-flop doesn't change condition simultaneously because it doesn't use single clock signal Also known as ripple counter because clock signal input as ripple through counter.
which type of counter is used in traffic signal?Ans.
Down counters.

EXPERIMENT NO: 8

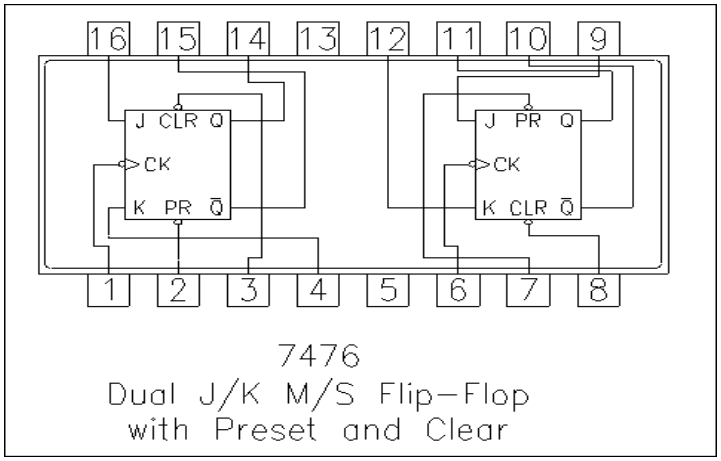
Aim: – Design, and Verify the 4-Bit Asynchronous Counter.

APPARATUS REQUIRED: Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

BRIEF THEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

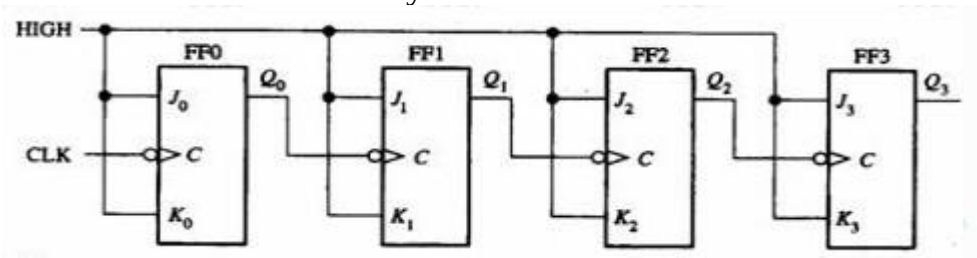
PIN CONFIGURATION:

Pin diagram of JK M/S Flip Flop



LOGIC DIAGRAM:

4-Bit Asynchronous counter



Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT: 4-bit asynchronous counter studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

How many flip-flops are required to make a MOD-32 binary counter?Ans. 5.

The terminal count of a modulus-11 binary counter is_____.

Ans.1010.
Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
Ans. Input clock pulses are applied simultaneously to each stage.

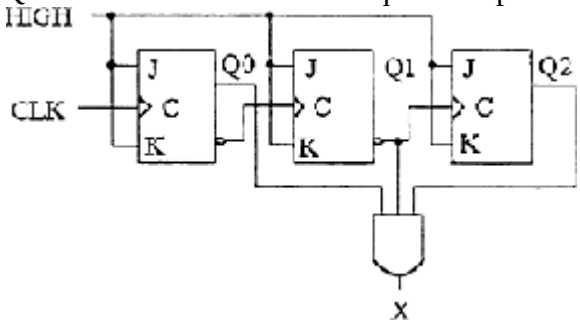
Q4. Synchronous construction reduces the delay time of a counter to the delay of:

Ans. a single flip-flop and a gate.

Q5. What is the difference between a 7490 and a 7492?

Ans.7490 is a MOD-10, 7492 is a MOD-12.

Q6. When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.
Ans. Product.
Q7. A BCD counter is a_____.
Ans. decade counter.
Q8. What decimal value is required to produce an output at "X" ?



Ans.5.

Q9. How many AND gates would be required to completely decode ALL the states of a MOD-64 counter, and how many inputs must each AND gate have?

Ans. 64 gates, 6 inputs to each gate.
Q.10 A ring counter consisting of five Flip-Flops will have
Ans. 5 states.

EXPERIMENT NO: 9

SILIGURI INSTITUTE OF TECHNOLGY

ELECTRONICS &COMMUNICATION ENGINEERING DEPARTMENT

DIGITAL SYSTEM DESIGN LAB.

PAPER CODE:EC392

AIM: Design and implementation of INVERTER Circuit using T-SPICE.

OBJECTIVE :

Design & Implementation of an INVERTER Circuit using T-SPICE.

THEORY:

Inverter is a circuit that inverts the input. When the input is high then the output will be low that means when input is 1 output is 0 and when the input is low the output will be high that means if input is 0, output will be 1.

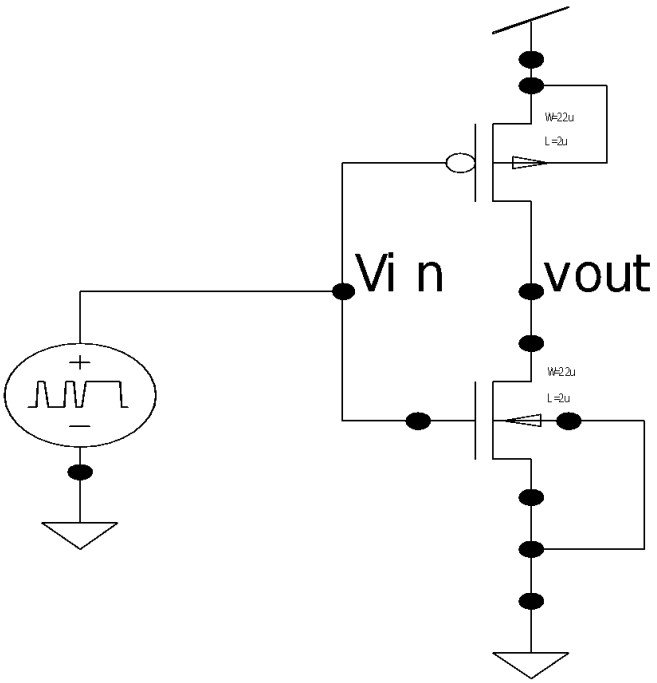
TRUTH TABLE :-

INPUT	OUTPUT
0	1
1	0

BOOLEAN EXPRESSION :

$Y = x'$

CIRCUIT DIAGRAM:



- **ANALYSIS/CIRCUIT DESCRIPTION:**

In this experiment, we have used CMOS logic design technique.

Here f = Vin'

So, f' = Vin

Now use f for pMOS circuit design & use f' for nMOS circuit design. Where boolean (.) indicate series operation and Boolean (+) signifies parallel operation. Based on this, we built the given circuit and simulate using TSPICE to observe the output waveform.

As per the above methodology one pMOS connected in series with an nMOS. Collecting output from their common node mentioned as V_{out}.

We gave two common inputs (V_{in}) to both the circuit parts.

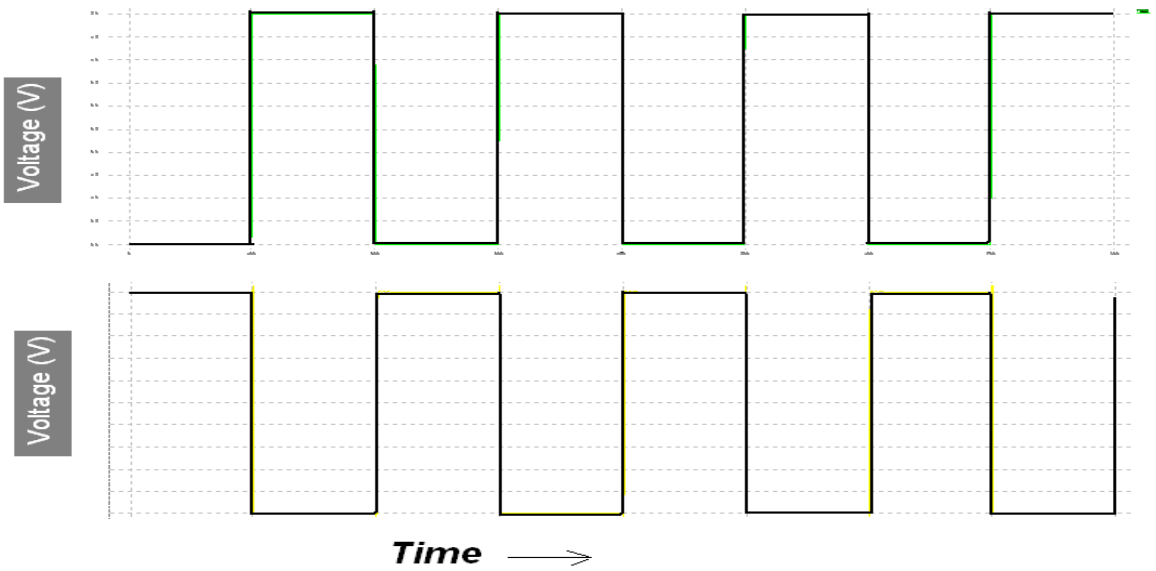
- **NETLIST :**

```
* Waveform probing commands
.probe
.options probefilename=" inverter.dat"
+ probesdbfile="D:\inverter.sdb"
+ probetopmodule ="inverter"

* Main circuit: inverter
M1 Vb Va Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 Vb Va Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
v3 Va Gnd bit({0101} pw=100n on=5.0 off=0.0 rt=1n ft=1n delay=0 lt=100n ht=100n)
.include "C:\Program Files\Tanner EDA\Demo\T-Spice\models\ml2_20.md"
Vdd Vdd Gnd 5v
.Tran 1n 800n
.print V(Vin),V(Vout)
```

- End of main circuit: inverter

OUTPUT WAVEFORM:



CONCLUSION:

After performing the above experiment we come to know about the operation of a NOT gate using T-SPICE .here we have performed the operation of a 1 input NOT gate which is basically a inverting operation of input. We have done dc & transient operation of the NOT gate. In the dc operation there is lots of noise interference in the output waveform which are eliminated in the transient operation by using source voltage bit instead of a dc input. As a result we got a output waveform as shown above.

EXPERIMENT NO :10

SILIGURI INSTITUTE OF TECHNOLGY

ELECTRONICS &COMMUNICATION ENGINEERING DEPARTMENT

DIGITAL SYSTEM DESIGN LAB.

PAPER CODE: EC392

AIM:- Design & Implementation of 8:1 Multiplexer circuit using VHDL

OBJECTIVE:- To design and implement a 8:1 Multiplexer using VHDL with the help of Xilinx ISE.

THEORY:-

Multiplexing is the process of transmitting a large number of information over a single line. A digital MUX is a combinational circuit that selects one

digital information from several sources and transmits the selected information on a single output line. A MUX is also called adata selector. The selection of of a particular input line is controlled by a set of select lines.

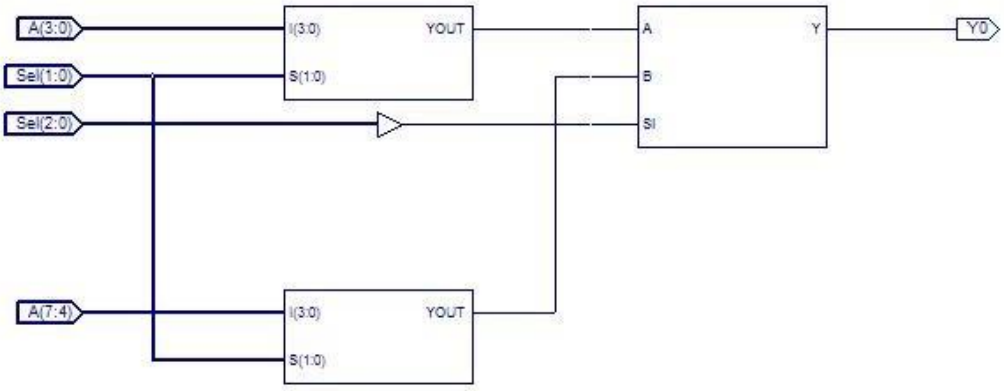
Truth table :-

INPUTS				OUTPUTS	
E’	S2	S1	S0	Y	Y’
1	X	X	X	1	0
0	0	0	0	D0	D0’
0	0	0	1	D1	D1’
0	0	1	0	D2	D2’
0	0	1	1	D3	D3’
0	1	0	0	D4	D4’
0	1	0	1	D5	D5’
0	1	1	0	D6	D6’
0	1	1	1	D7	D7’

Boolean Expression:-

Y=ABCD+AB'CD+A'B'CD+A'BC'D+A'B'C'D+ABCD'+A'BCD'+ AB'CD'+A'BC'D'+AB'C'D'

SCHEMATIC DIAGRAM OF THE CIRCUIT:-



VHDL PROGRAM:-

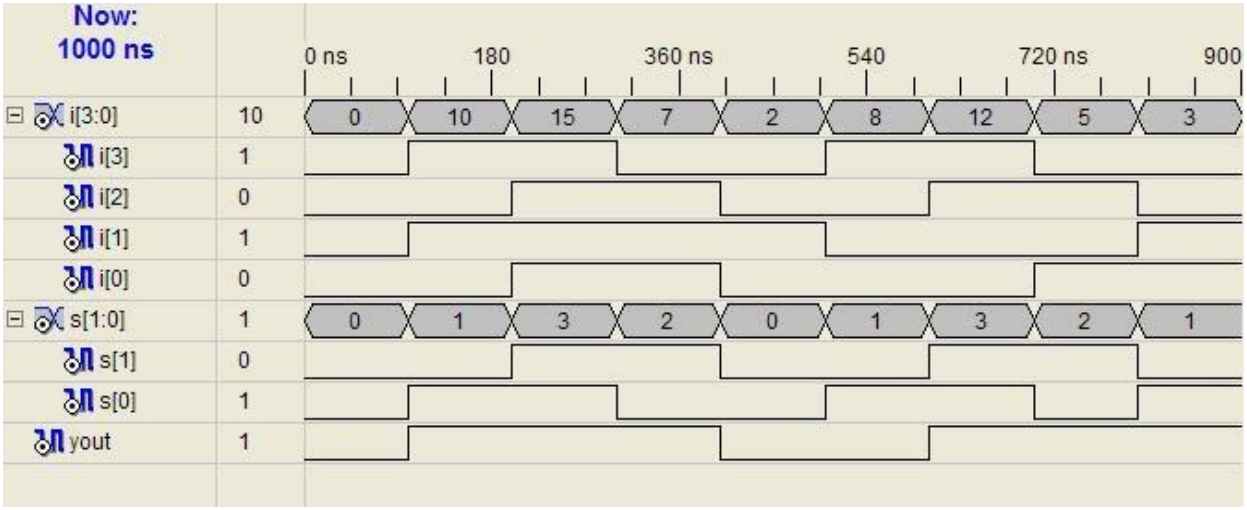
```
Port ( Sl,A,B : in std_logic;
        Y : out std_logic);
       end Component;

     Component mux4_1 is
     Port ( I : in std_logic_vector(3 downto 0);
     S : in std_logic_vector(1 downto 0);
     YOUT : out std_logic);
       end Component;

begin
        L1:mux4_1 port map(A(7 downto 4),Sel(1 downto 0),Sig0);
        L2:mux4_1 port map(A(3 downto 0),Sel(1 downto 0),Sig1);
        L3:mux2_1 port map(Sel(2),Sig1,Sig0,Y0);
```

end Structure;

OUTPUT WAVEFORM:-



CONCLUSION:-

A Multiplexer is a combinational circuit thar selects one digital information from several sources and transmits the selected information on a single output line with the help of a set of selection lines. Any Boolean or Logical expression can be easily implemented using a multiplexer. If a Boolean Expression has (n+1) variables then n of these variables can be connected to the select lines of a multiplexer. Here we have used the Structural process to build the program for 8:1 Multiplexer in Xilinx ISE.

EXPERIMENT NO: 11

SILIGURI INSTITUTE OF TECHNOLGY

ELECTRONICS &COMMUNICATION ENGINEERING DEPARTMENT

DIGITAL SYSTEM DESIGN LAB.

PAPER CODE:EC 392

AIM:

Design and implementation of CMOS T-SPICE

OBJECTIVE:-

To design and implementation of a two input NAND gate using TSPICE and analyze the Transient characteristics of output waveform.

THEORY:

If we take Va as 1st input of the NAND gate, & Vb as 2nd input of the NAND gate then output can be expressed as-

Vout = (Va.Vb)'.

Which may also be expressed as- Vout = (Va.Vb)' = Va'+Vb'.

It must be noted as the output of this circuit is just the opposite of AND gate (initially observed).

TRUTH TABLE:

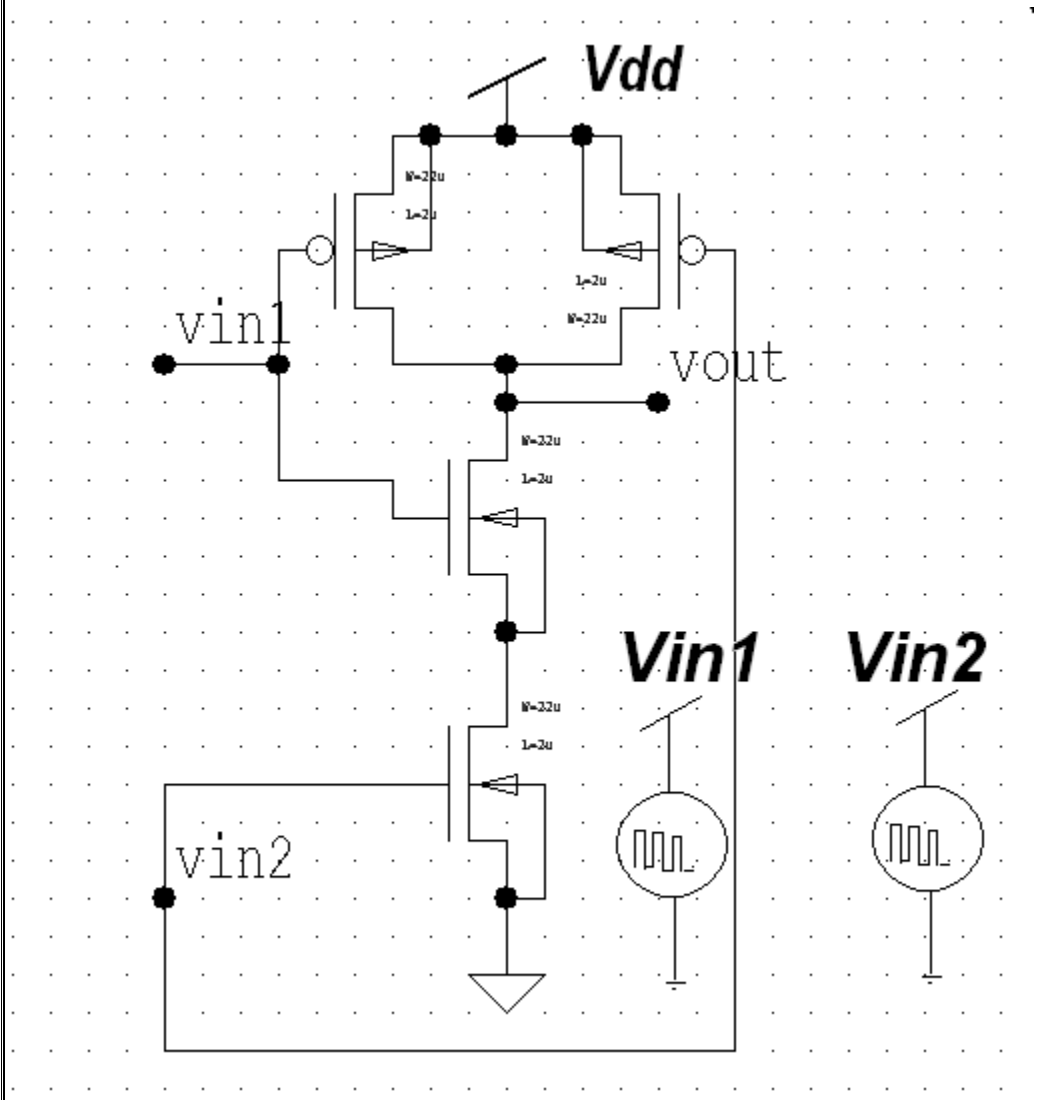
Va	Vb	Va.Vb	(Va.Vb)'
0	0	0	1
0	1	0	1

1	0	0	1
1	1	1	0

BOOLEAN EXPRESSION:

Vout = (Va.Vb)' = Va' + Vb'.

SCHEMATIC DIAGRAM OF THE CIRCUIT:



CIRCUIT DESCRIPTION:

In this experiment, we have used CMOS logic design technique.

Here f = (Va.Vb)'=Va' +Vb'

So, f' = ((Va.Vb)')'=Va.Vb

Now use f for pMOS circuit design & use f' for nMOS circuit design. Where boolean (.) indicate series operation and Boolean (+) signifies parallel operation.Based on this, we built the given circuit and simulate using TSPICE to observe the output waveform.

As per the above methodology two pMOS connected in parallel and two nMOS connected in series. Collecting output from their common node mentioned as Vout.

We gave two common inputs (Va and Vb) to both the circuit parts.

NETLIST:

```
* SPICE netlist written by S-Edit Win32 Demo 9.12
* Written on Apr 2, 2009 at 10:45:05

* Waveform probing commands

.probe
.options probefilename="NAND_GATE.dat"
+ probesdbfile="G:\ NAND_GATE.sdb"
+ probetopmodule=" NAND_GATE"

* Main circuit: NAND_GATE
```

```
M1 vout vin1 N2 N2 NMOS L=2u W=44u AD=66p PD=24u AS=66p PS=24u
M2 N2 vin2 Gnd Gnd NMOS L=2u W=44u AD=66p PD=24u AS=66p PS=24u
M3 vout vin1 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M4 Vdd vin2 vout Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
v5 vin1 Gnd bit ({0100} pw=100n on=5.0 off=0.0 rt=1n ft=1n delay=0 lt=100n ht=100n)
v6 vin2 Gnd bit ({1111} pw=100n on=5.0 off=0.0 rt=1n ft=1n delay=0 lt=100n ht=100n)

.include "C:\Program Files\Tanner EDA\Demo\T-Spice\models\ml2_125.md"
vdd vdd gnd 5

.tran 1n 400n


.print tran v(vin1) v(vin2) v(vout)
```

OUTPUT WAVEFORM:

CONCLUSION:

After performing the above experiment we come to know about the operation of a NAND gate using T-SPICE .here we have performed the operation of a 2 input NAND gate which is basically a multiplication operation between two inputs. We have done dc & transient operation of the NAND gate. In the dc operation there is lots of noise interference in the output waveform which are eliminated in the transient operation by using source voltage bit instead of a dc input. As a result we got an output waveform as shown above.

EC 492 ANALOG ELECTRONIC CIRCUITS LAB

LABORATORY MANUAL

SEMESTER III

DEAPRTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

Maulana Abul Kalam Azad University of Technology, West Bengal

(Formerly West Bengal University of Technology)

Syllabus for B. Tech in Electronics & Communication Engineering

(Applicable from the academic session 2018-2019)

Course Code : EC 492 **Category :** Core Courses

Course Title : Analog Electronic Circuits Lab	**Semester** : Four
L-T-P : **0-0-2**	**Credit:1**

Detailed contents:

1. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).

2. Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency:

(a). Full Wave Rectifier (b). Bridge Rectifier

3.Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.

4. Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency

5. Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances

6. Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.

7. Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.

(a) Hartley Oscillator (b) Colpitts Oscillator

8. Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.

9. Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.

Course Outcome:

Students will be able to:

CO1: Design and test rectifiers, clipping circuits, clamping circuits and voltage regulators.

CO2: Compute the parameters from the characteristics of JFET and MOSFET devices.

CO3: Design, test and evaluate BJT amplifiers in CE configuration.

CO4: Design and test JFET/MOSFET amplifiers.

CO5: Design and test a power amplifier.

CO6: Design and test various types of oscillators.

Contents

SILIGURI INSTITUTE OF TECHNOLOGY

DEPT. OF E.C.E

Paper Code: EC 492 **Course Title : Analog Electronic Circuits Lab**

Experiment No.: 1 **Date:**

AIM

To design and implement diode clipping circuits.

OBJECTIVE

The purpose of this lab is to introduce students to design and implement following diode clipping circuits.

i) Negative series clipper
ii) Positive series clipper
iii) Negative shunt clipper
iv) Positive shunt clipper
v) Biased negative shunt clipper
vi) Biased positive shunt clipper
vii) Biased negative and positive shunt clipper

THEORY

Diode clipping circuits

The function of a clipper (or limiter) is to limit an ac voltage to predetermined level. This is sometimes necessary to protect a device or circuit that might be destroyed by large amplitude (negative or positive) signal. Limiters can transform a sine wave into a square wave; and can perform other useful wave shaping functions.

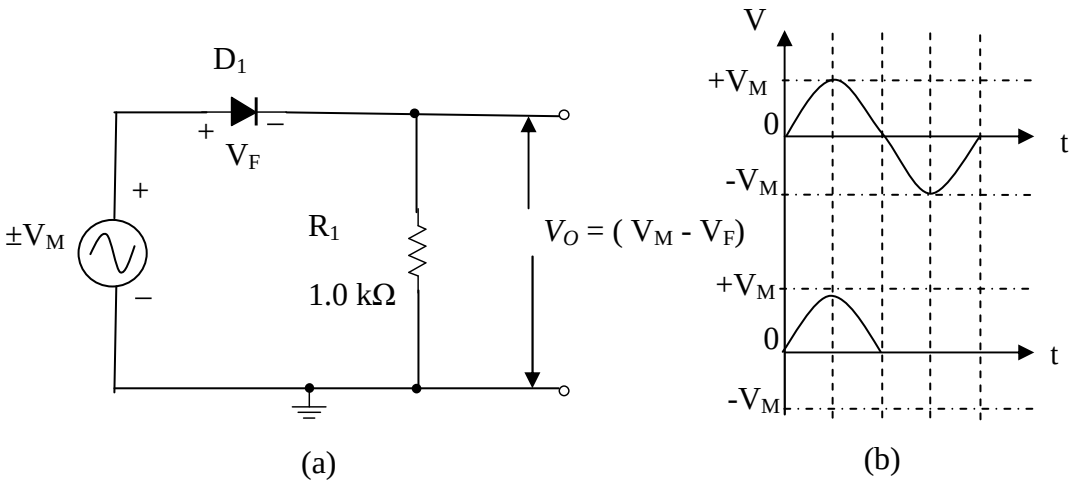


Fig. 1(a): Negative series clipper, (b): input and output waveforms.

(a) Negative series clipper: Figure 1(a) shows a negative series clipper circuit with ac input signal. It is called series limiter because the output is taken from the load resister R1 is in series with the diode. While the input is positive D1 is forward biased and the positive half cycle is passed to the output. The peak output voltage

$$\mathbf{V_{PO} = V_{PI} - V_F}$$

Where V_{PI} is the peak input voltage and V_F is the diode forward voltage drop. During negative half cycle of input, the diode is reversed biased. Consequently the output remains zero and the negative half-cycle is effectively clipped off.

The output terminals of series clippers are usually connected to circuits that have high input resistance, so resistor R_1 (current limiting resistor) is selected to pass an acceptable minimum current through the diode. Typically a current of 1 mA is appropriate to be sufficient to operate the diode beyond the knee of its forward characteristics.

Design problem

Design a negative series clipper (Fig. 1(a)) sinusoidal input voltage ±9 V (p-p) and zero load current. Determine a suitable resistor R_1 and specify the diode forward current and reverse voltage. (Use silicon diode).

Solution: $V_{PO} = V_{PI} - V_F$

= 9 – 0.7 V

= 8.3 V

Select $I_F = 1$ mA

This implies $R_1 = V_{PO} / I_F$

= 8.3 V/ 1mA

= 8.3 kΩ (use 8.2 kΩ standard value)

(b) Positive series clipper

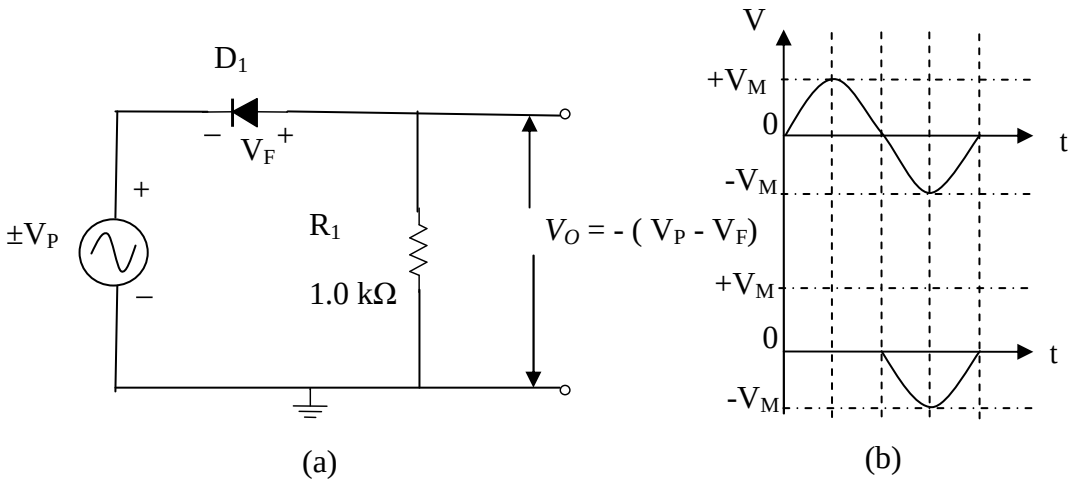


Fig. 2(a): Positive series clipper, (b): input and output waveforms.

If the diode in Fig.1 (a) is reconnected with reversed polarity, as shown in Fig 2(a), the positive series half-cycles are clipped off, and the circuit becomes a positive series clipper. The input waveforms to a clipper may be a square, or sinusoidal, or any other shape.

The design process to find the value of resistor R1 and diode specification is same as given in the negative series clipper.

Shunt clipper circuits

(a) Positive shunt clipper: A positive shunt (parallel) clipper is shown in Figure 3(a). Here the diode is connected in parallel with the output terminals. During negative half-cycles of the input signal the diode is reversed biased and only a small voltage drop occurs across R1 due to load current I_L. Hence the circuit output voltage (V_O) is

approximately equal to the negative input peak ($-V_{in}$). When the input is $+V_M$, D_1 is forward biased, and the output voltage equals the diode voltage drop (V_F). Thus positive half-cycles of the waveform are clipped off. As illustrated, upper and lower levels of the output of a positive shunt clipper are approximately $+V_F$ and $-V_M$.

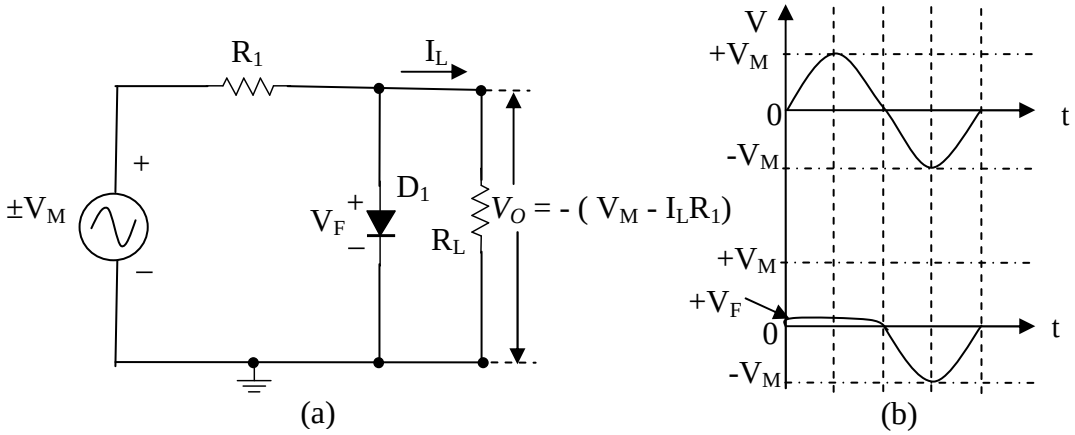


Fig. 3(a): Positive shunt clipper, (b): input and output waveforms.

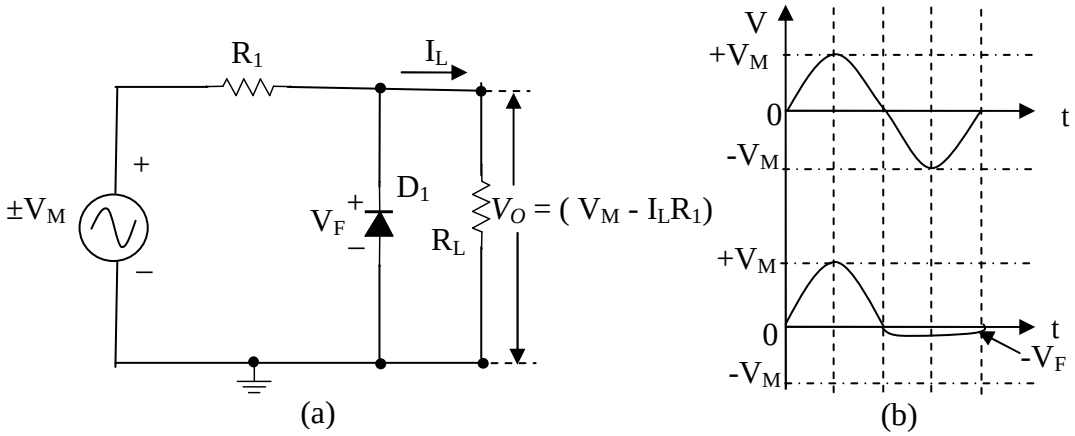


Fig. 4(a): Negative shunt clipper, (b): input and output waveforms.

(b) Negative shunt clipper: A negative shunt clipper circuit is exactly the same as a positive shunt clipper with the diode polarity reversed, [Fig 4(a) and (b)]. The negative half-cycles of the waveform are clipped off.

The load current on a shunt clipper produces a voltage drop (I_LR_1) across the resistor, which might be insignificant where the load current is very low.

$$\mathbf{V_O = V_M - (I_LR_1)}$$

As in the series clipping circuits, shunt clippers may be used with square, sinusoidal, or any other waveforms.

Design problem

The negative shunt clipper in figure 4(a) has a ± 9 V input, and is to produce a +5 V minimum output when the load current is 2 mA. Determine a suitable resistance for R_1, and specify the diode forward current and reverse voltage.

Solution

When the Diode D_1 in figure 4(a) is reversed biased,

$$V_O = V_M - (I_L R_1)$$

or, $$R_1 = \frac{V_M - V_O}{I_L} = \frac{9-5}{2\times10^{-3}}\Omega = 2k\Omega$$ (2.2kΩ may be used)

Diode reverse voltage,

$$V_R = V_M = 9V$$

When the diode is forward biased,

$$I_F = \frac{V_M - V_F}{R_1} = \frac{9-0.7}{2.2\times10^3} A = 3.8mA$$

(c) Biased negative shunt clipper: Figure 5(a) shows a negative shunt clipping circuit that uses a DC supply V_B in series with the diode D_1. The circuit accomplishes partial clipping of the negative half-cycles of an input sine wave.

Diode D_1 in figure 5(a) is reverse-biased by DC supply V_B which maintains the anode V_B volts negative relative to its cathode. During the positive half-cycles of the input voltage V_{in}, the cathode of D_1 is held positive .The diode acts as an open switch, and the positive half-cycles passes in the output [figure 5(b)]. During the negative half-cycles the cathode is driven negative, but the diode will not conduct until V_{in} is more negative than the bias voltage V_B which maintains the anode V_B volts negative. Hence, that part of the negative alteration which is less negative than V_B appears in the output. When the

negative half cycle of Vin reaches the level where it is more negative than V_B, the cathode is driven more negative than the anode and the diode conducts, limit5ing that portion between $-V_B$ [precisely $-(V_B + V_F)$] and $-V_M$ peak. The input and output waveform is shown in figure 5(b).

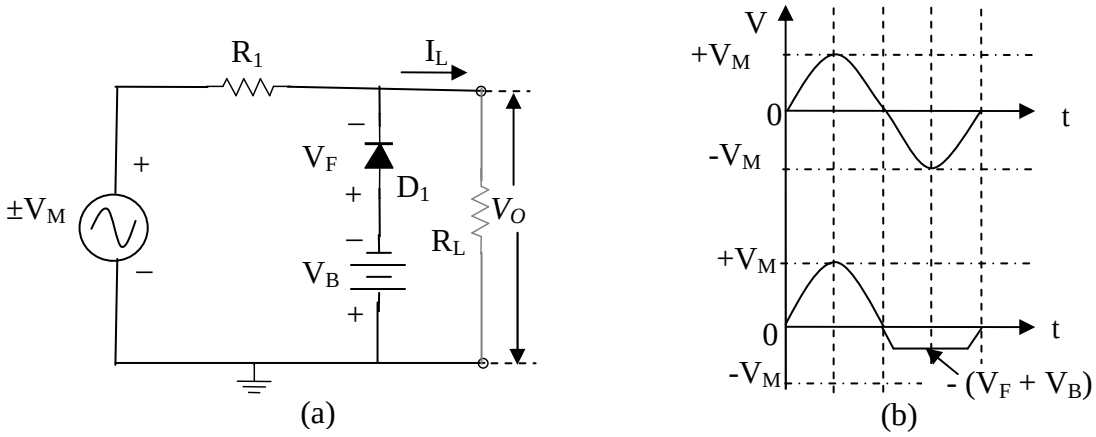


Fig. 5(a): Biased negative shunt clipper, (b): input and output waveforms.

(d) Biased Positive shunt clipper: Figure 6(a) and (b) shows the circuit and input-output waveforms of a biased positive shunt clipper. It is exactly the same as a biased negative shunt clipper with the diode and DC supply polarity reversed as shown in the figure.

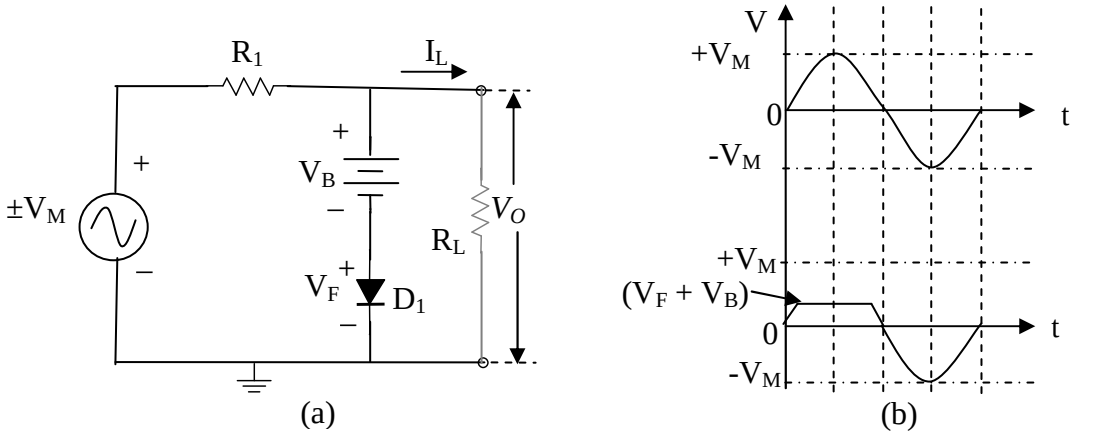


Fig. 6(a): Biased positive shunt clipper, (b): input and output waveforms.

(e) Biased double diode shunt clipper: figure 7(a) and (b) shows the circuit and input-output waveforms of a biased double diode shunt clipper. The circuit uses two diodes

which have different bias voltages as shown in the figure. While the input waveform amplitude is less than ± (V_B +V_F), neither diode is forward biased, and the input is simply passed to the output. When the positive input is greater than (V_{B1} + V_F), diode D_1 is forward biased, and the output can not exceed this voltage. Similarly, when the negative input goes below (- V_{B2} - V_F), D_2 is forward biased, and the output is limited to – (V_{B2} + V_F).

$$\mathbf{V_O = \pm (V_B + V_F)}$$

Biased shunt clippers are used to protect circuits or devices from (positive/negative) input voltages that must not exceed specified levels. The voltage across resistor R_1 is (V_M – V_O), and the resistor current is the sum of the load current and the diode forward current (I_L + I_F). As in the diode circuits, a minimum level of I_F is selected, and resistor value is calculated as,

$$R_1 = \frac{V_M - V_O}{I_L + I_F}$$

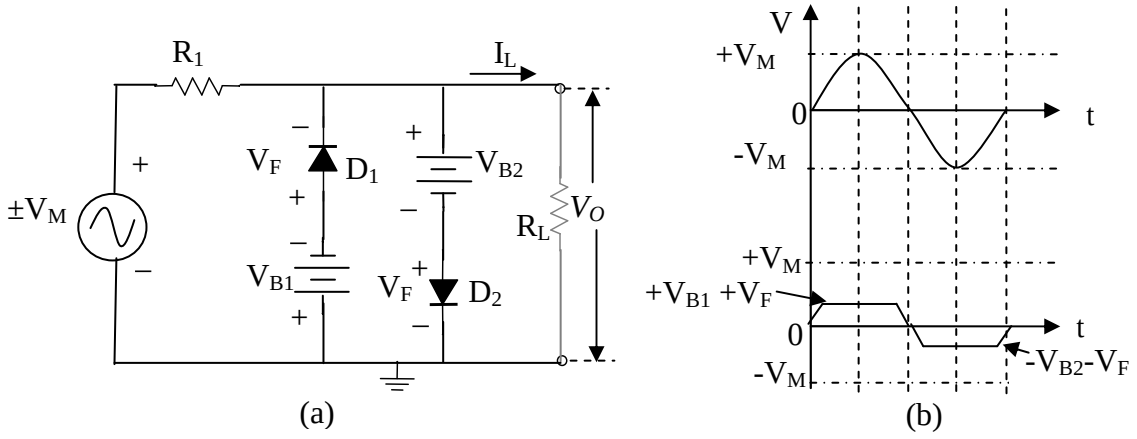


Fig. 7(a): Biased double diode shunt clipper, (b): input and output waveforms.

Design problem:

The biased shunt clipper in figure 7(a) has a ±9 V input, and its output is to be limited to ± 5 V. Determine a suitable resistance for R_1 if the clipper output current is to be ±1 mA.

Solution:

$$V_O = \pm (V_B + V_F)$$

Giving, $$V_B = \pm (V_O - V_F)$$

$$= \pm (5\ V - 0.7\ V)$$

$$= \pm 4.3\ V$$

Select the diode forward current as,

$$I_F = 1\ mA$$

Then $$R_1 = \frac{V_M - V_O}{I_L + I_F} = \frac{9V - 5V}{1mA + 1mA}$$

$$= 2\ k\Omega\ (2.2\ k\Omega \text{ can be used})$$

APPARATUS REQUIRED

Sr. No.	Components	Quantity
1.	Variable regulated DC power source	2
2.	Signal generator	1
3.	Diode 1N4007	2
4.	Resistor 470 kΩ	1
5.	Resistor 2 kΩ or 2.2 kΩ	1
6.	Breadboard	1
7.	Dual trace CRO	1
8.	Digital Multimeter	1
9.	Connecting wires and patch cords	1 m

PROCEDURE

1. According to the design problem, find the values of components. Rig the circuit on a breadboard.
2. Connect the DC voltage source, signal generator and CRO according to the circuit diagram.

3. Switch on the circuit and observe the input and output waveforms on the CRO screen and plot it on a graph sheet.

CIRCUIT DIAGRAM AND OBSERVATIONS

Negative series clipper

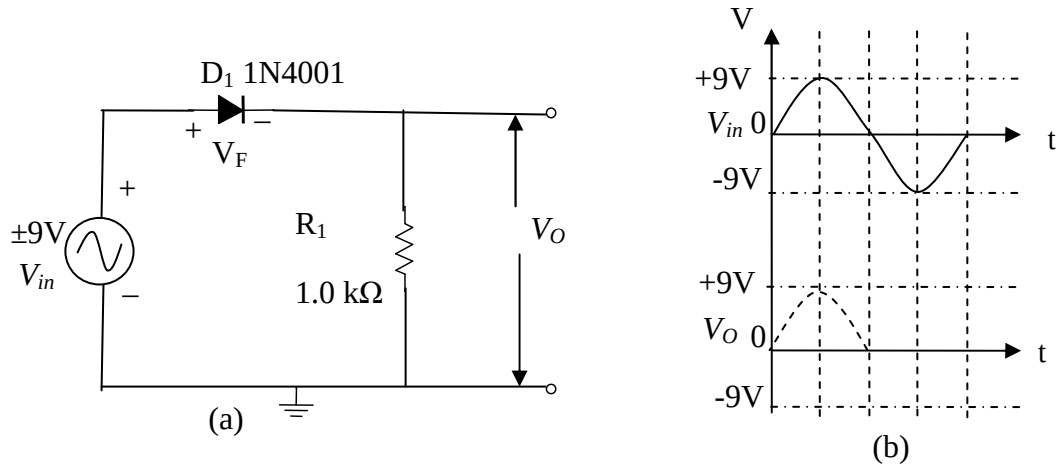


Fig.:8.(a) Negative series clipper; (b): input and output waveforms.

Positive series clipper

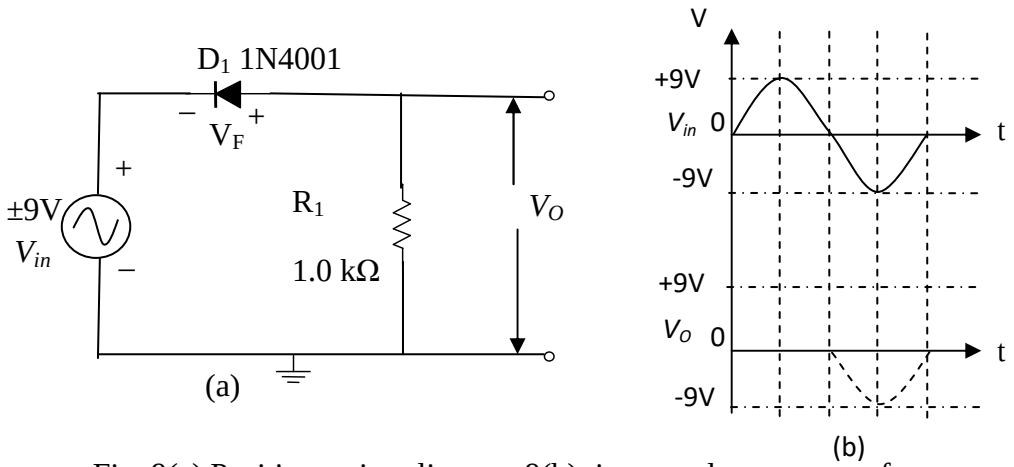
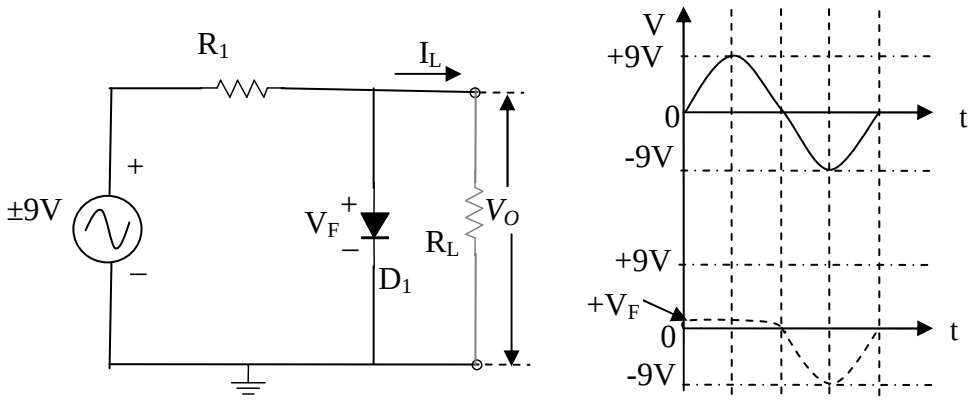


Fig. 9(a) Positive series clipper; 9(b): input and output waveforms.

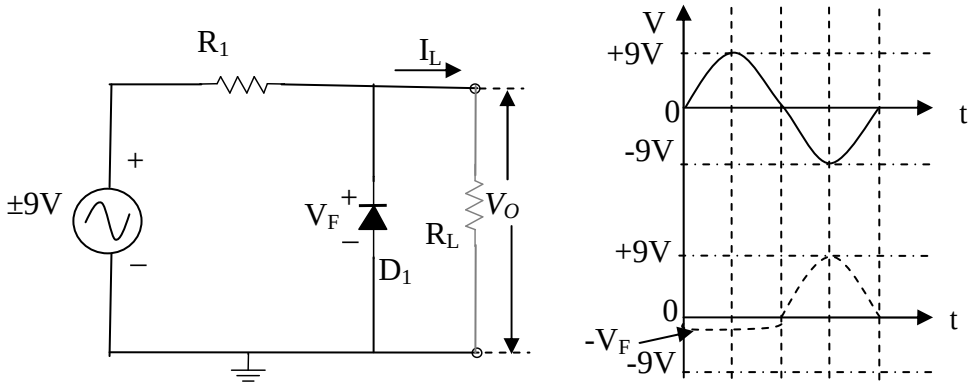
Positive shunt clipper



(a) (b)

Fig. 3(a): Positive shunt clipper, (b): input and output waveforms.

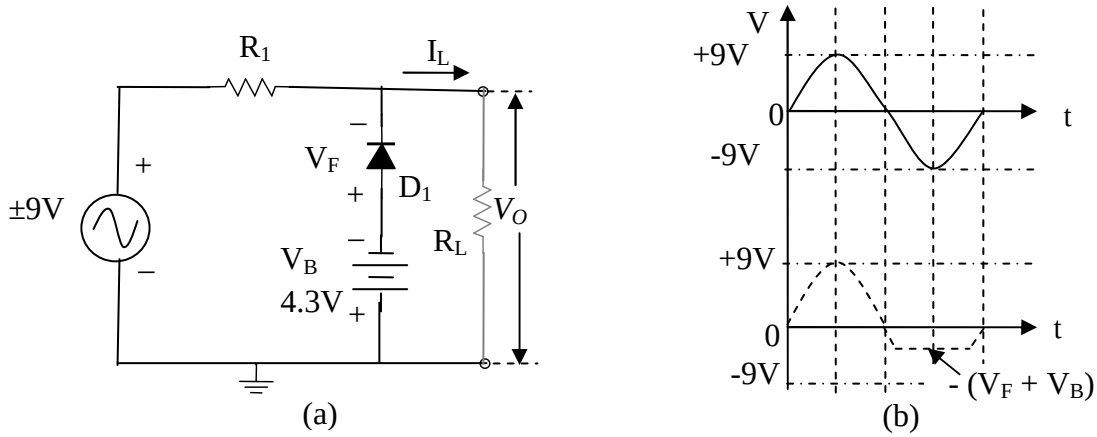
Negative shunt clipper



(a) (b)

Fig. 3(a): Negative shunt clipper, (b): input and output waveforms.

Biased negative shunt clipper



(a) (b)

Fig. 5(a): Biased negative shunt clipper, (b): input and output waveforms.

Biased positive shunt clipper

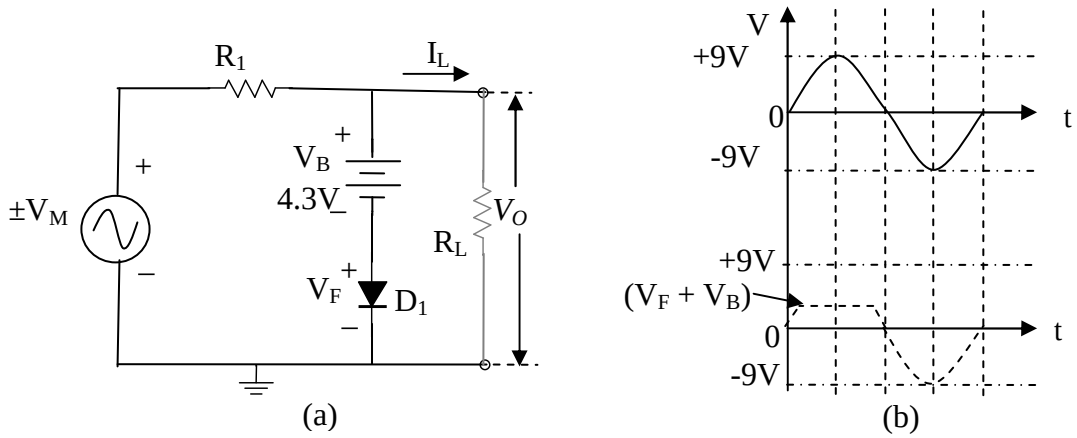


Fig. 6(a): Biased positive shunt clipper, (b): input and output waveforms.

Biased double diode shunt clipper

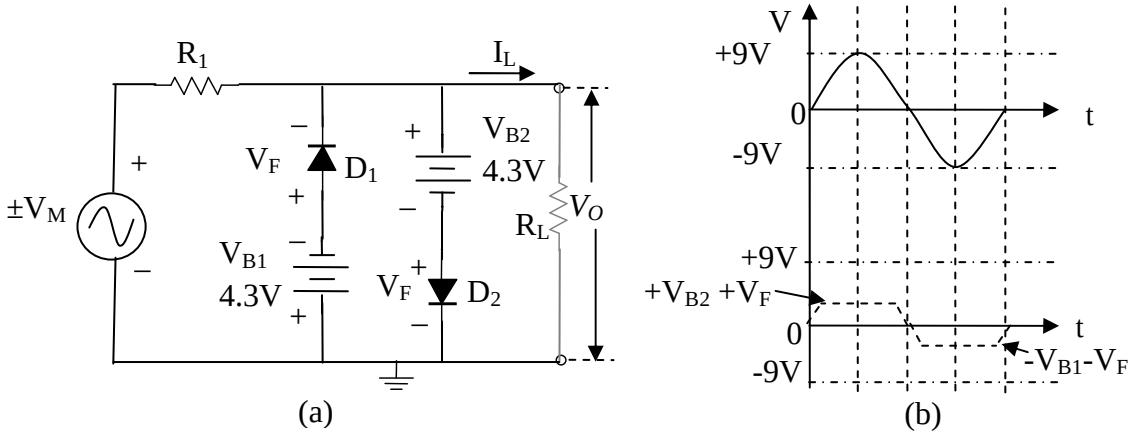


Fig. 7(a): Biased double diode shunt clipper, (b): input and output waveforms.

CONCLUSION

SILIGURI INSTITUTE OF TECHNOLOGY

DEPT. OF E.C.E

Paper Code: EC 492 **Course Title: Analog Electronic Circuits Lab**

Experiment No.: 2 **Date:**

AIM

To design and implement Negative and Positive Diode Clamping Circuits

OBJECTIVE

The purpose of this experiment is to introduce students to design and implement following diode clamping circuits.

a) Negative voltage clamper
b) Positive voltage clamper

THEORY

A clamping circuit changes the dc voltage level of a waveform, but does not affect its shape. In other words, in steady state, the output waveform is an exact replica of the input waveform, but the output signal is shifted by a dc value that depends on the circuit.

Negative Voltage Clamping Circuit

A negative voltage clamping circuit is shown in Fig.1 (a).

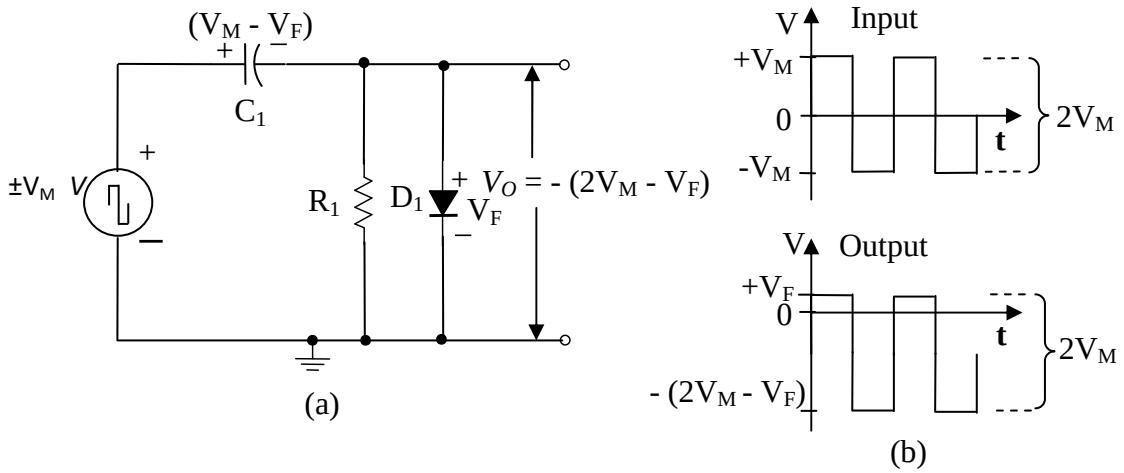


Fig. 1(a): A Negative voltage clamping circuit, (b): Input and Output waveforms.

During the positive half cycle of the square wave input, diode D_1 is forward biased, and the output voltage equals the diode forward voltage drop (V_F).

$$V_O = V_F$$

Also, during positive half cycle of the input, the capacitor C_1 is charged with the polarity shown to a voltage,

$$V_C = (V_M - V_F)$$

During the negative half cycle of the input the diode D_1 is reversed biased and has no further effect on the capacitor voltage. Also, the R_1 has very high resistance, so it cannot discharge C_1 significantly during negative portion of the input waveform. During this half cycle polarity of the capacitor voltage is same as the (negative) input, the output is,

$$V_O = - (V_M + V_C)$$

$$= - [(V_M + (V_M - V_F \quad)]$$

or, $\mathbf{V_O = - (2V_M - V_F)}$

Also we can find, $\mathbf{V_{O(P\text{-}P)} = 2\ V_M}$

The output waveform of the **negative voltage clamping circuit** is (almost) completely negative and the **output positive peak clamped at a level of $+V_F$**.

Positive Voltage Clamping Circuit

We can design a positive voltage clamping circuit shown in fig. 2(a) by reversing the polarity of the diode and capacitor of a negative voltage clamping circuit.

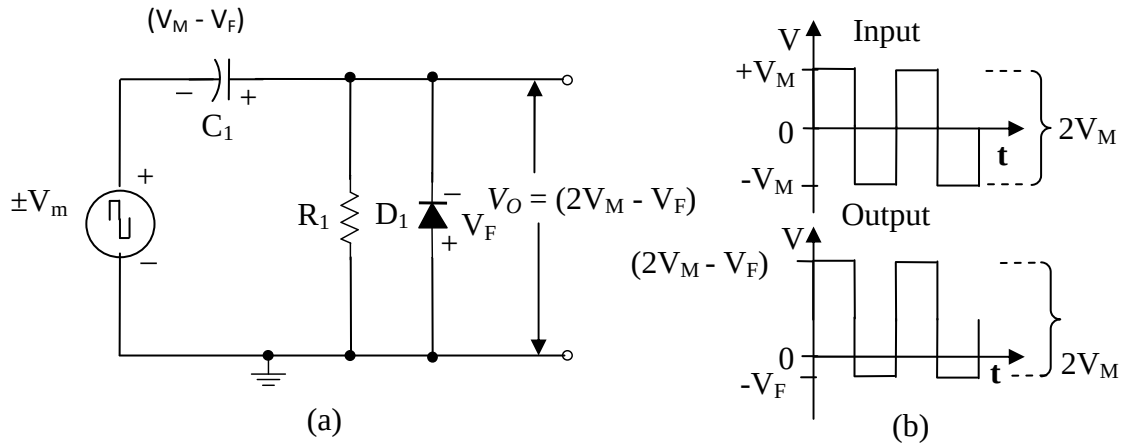


Fig. 2(a): A Positive voltage clamping circuit, (b): Input and Output waveforms.

As illustrated, the output waveform of a **positive clamping circuit** is clamped to keep it (almost) completely positive. In other words a positive clamping circuit passes the complete input waveform to the output, but clamps the negative peak of the output close the ground level.

Output Slope

Resistor R_1 in figure 1(a) and 2(a) is sometimes termed as bleeder resistor. It is used to gradually discharge the capacitor C_1 over several cycles of input waveform, so that it can be charged to new level when the input changes. However, R_1 partially discharges the capacitor during the time when D_1 is reversed biased. This produces a slope or tilt (ΔV_C) on the output waveform, as shown in Fig.3.

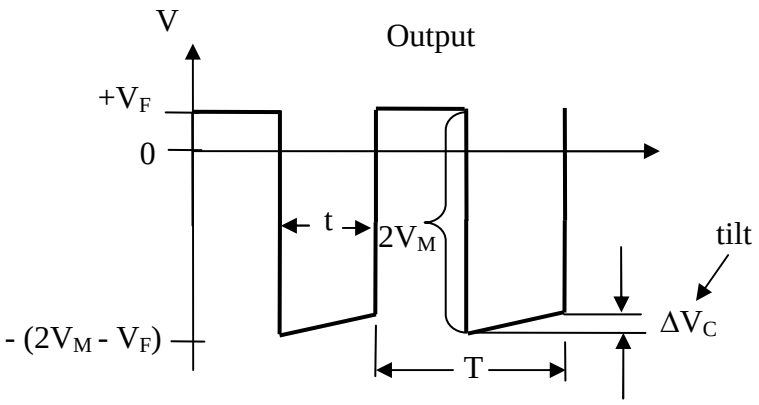


Fig. 3: The output voltage from a clamping circuit has a slope (ΔV_C) produced by capacitor discharge.

Design Problem

Design a negative voltage clamping circuit as shown in Fig.1 (a). It has a ±10 V, 1 KHz square wave input with a 50 Ω signal source resistance. The output waveform should have maximum slope (ΔV_C) of 5%. Determine suitable values of R_1 and C_1.

Solution

$t = T/2 = 1/2f_o$ ($T = 1/f_o$)

$= 1/(2 \times 1000\ Hz) = 0.5$ ms

Hence, Pulse width, PW = t = 0.5 ms

Since, PW or $t = C_1 \times R_S$ (A capacitor is completely charged in approximately five time constants of the circuit. In the case of a R-C circuit, the time constant is RC. So, 5 RC = 5 PW or PW = RC)

$C_1 = PW/R_S = 0.5$ ms /50Ω [$(0.5 \times 10^{-3})/ 50 = 10 \times 10^{-6}$]

$= 10\ \mu F$

$V_{O(pp)} = 2V_M = 2 \times 10$ V (since, $V_M = 10$ V)

$= 20$ V

ΔV_C = 5% of $V_{O(pp)}$ = 5% of 20 V

= 1V

We know, $\Delta V_C = (I_C \times t)/C_1$ $\{\Delta V = \Delta Q/C\}$

Hence, $I_C = (\Delta V_C \times C_1)/ t = (1\ V \times 10\mu F)/0.5\ ms$

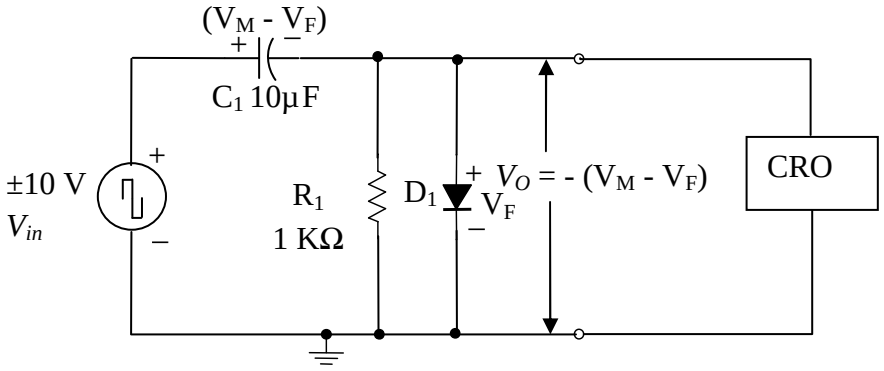
= 20mA

Since, $I_C = V_O/R_1$ and $V_O = 2V_M$

$R_1 = 20\ V/20\ mA$

= 1KΩ

Use 1N4007 as diode D_1. The designed circuit is shown in Fig.4.



(a)

Fig. 4: A Negative voltage clamping circuit (designed)

Apparatus and Components Required

Sr. No.	Components	Quantity
1.	Signal generator	01
2.	20 MHz Dual trace CRO/DSO	01
3.	DMM	01
4.	Breadboard	01
5.	Diode 1N4007	01

6.	Resistor 1 kΩ 0.25 W	01
7.	Capacitor 10 μF , 50V	01
8.	Hook up Wire 24 or 25 SWG	1 m

Observation table 1: Positive Diode Clamper circuit

$V_{IN(P-P)}$ (V)	ΔV_C (calculated) (V)	ΔV_C (observed) (V)	V_O (calculated) (V)	V_O (Observed) (V)

Observation table 2: Negative Diode Clamper circuit

$V_{IN(P-P)}$ (V)	ΔV_C (calculated) (V)	ΔV_C (observed) (V)	V_O (calculated) (V)	V_O (Observed) (V)

PROCEDURE

4. According to the design problem, find the values of components. Rig the circuit on a breadboard.
5. Connect the Signal generator and CRO according to the circuit diagram.
6. Apply 20 V peak to peak square wave as input from the signal generator.
7. Observe the input and output waveforms on the CRO screen. Record the different voltages of the waveforms in the observation table and plot it on a graph sheet.

Calculations:

Conclusion:

SILIGURI INSTITUTE OF TECHNOLOGY

DEPT. OF E.C.E

Paper Code: EC 492 **Course Title : Analog Electronic Circuits Lab**

Experiment No.: 3 **Date:**

AIM: To design and implement of a full wave bridge rectifier circuit with and without filter.

OBJECTIVE:

1. To design and implement afull wave rectifier circuit.
2. To study the ripple factor, percentage of regulation, input and output waveform of a full wave rectifier without filter and with capacitive input filter.

APPARATUS REQUIRED:

Sl. No.	Name Of The Apparatus	Specification/Range	Quantity
1.	Bread Board		01
2.	Step down transformer	220V AC to 0 – 6V, 300 mA	01
3.	Diode 1N4007		01
4.	Resistor	200 Ω, ¼ W	01
5.	Capacitor	470µF, 50 V	01
6.	DMM		01
7.	Single Strand Wire	25 or 26 SWG	1 m
8.	CRO or DSO	DC to 20 MHz	01

Theory:

A device is capable of converting a sinusoidal input waveform into a unidirectional waveform with non zero average component is called a rectifier. The Bridge rectifier is a circuit, which converts an ac voltage to dc voltage using both half cycles of the input ac voltage. The Bridge rectifier has four diodes connected to form a Bridge. The load resistance is connected between the other two ends of the bridge.

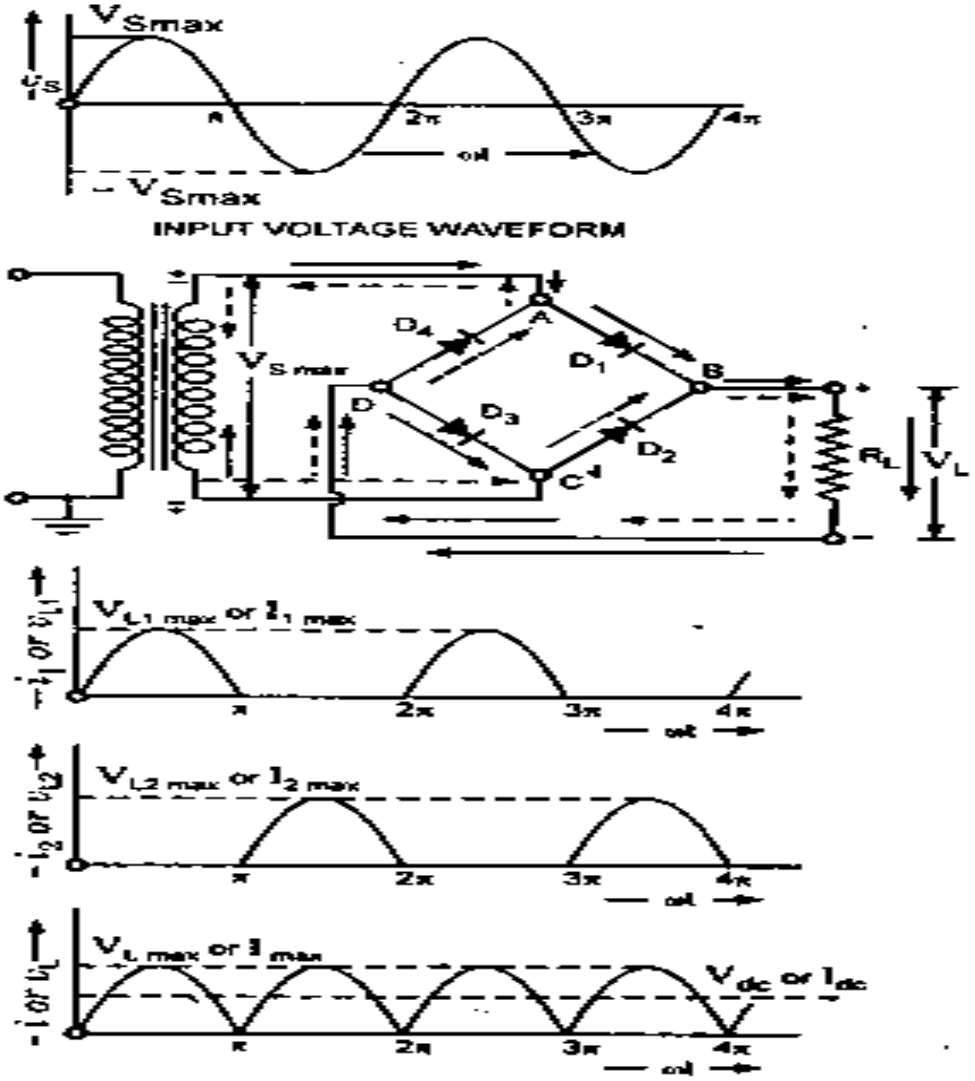
For the positive half cycle of the input ac voltage, diode D_1 and D_3 conducts whereas diodes D_2 and D_4 remain in the OFF state. The conducting diodes will be in series with the

load resistance R_L and hence the load current flows through R_L. For the negative half cycle of the input ac voltage, diode D_2 and D_4 conducts whereas diodes D_1 and D_3 remain in the OFF state.

The conducting diodes will be in series with the load resistance R_L and hence the load current flows through R_L in the same direction as in the previous half cycle. Thus a bidirectional wave is converted into a unidirectional wave. Ripple factor is a measure of effectiveness of a rectifier circuit and defined as a ratio of RMS value of ac component to the dc component in the rectifier output.

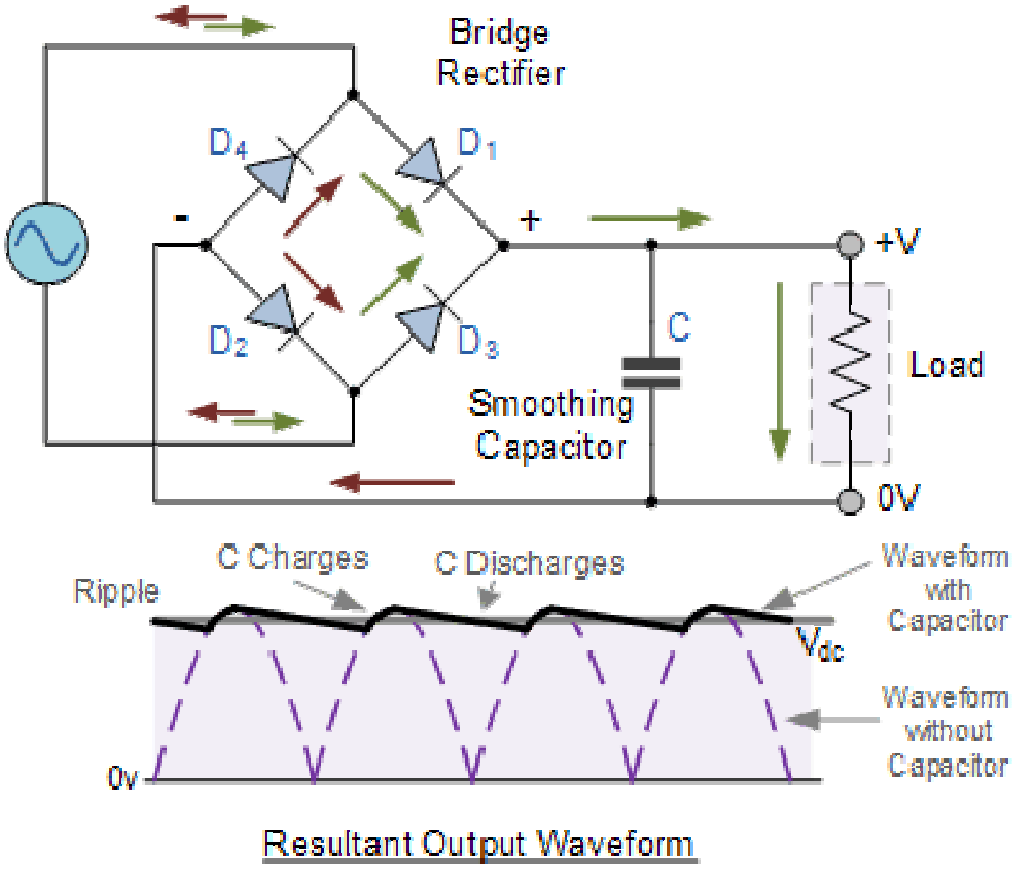
CIRCUIT DIAGRAM:

Full wave bridge rectifier circuit without filter capacitor



Bridge Rectifier

Full wave bridge rectifier circuit with filter capacitor



DESIGN PROBLEM: Design a full wave bridge rectifier with capacitive input filter to produce an output dc voltage 5.5 V when load current is 30 mA and ripple factor is 0.03. Find out the value of load resistor R_L and filter C.

SOLUTION:

Given, $V_{dc} = 5.5$ V, $I_L = 30$ mA, $\Gamma = 0.03$

As we know, $V_{dc} = 2V_m/\pi$

$V_m = \pi V_{dc}/2 = 5.5\pi/2$

$= 8.64$ V

$V_{dc} = I_L.R_L$

$R_L = 5.5$ V/30 mA = 183 Ω. Choose $R_L = 200$ Ω

$V_{rms} = V_m/\sqrt{2} = 8.64/\sqrt{2}$

$= 6.11$ V Use step down transformer with secondary voltage 6 V.

$\Gamma = 1/(4\sqrt{3} f_o CR_L)$

$C = 1/(4\sqrt{3} f_o \Gamma R_L)$ f_o = 50 Hz , the line frequency

C = 481 µF . Choose 470µF as the nearest standard value

OBSERVATION TABLE:

1) Observation Of Rectified Output using DMM :

Type Of Rectifier Circuit	**V_{dc} (V)**	**V_{ac} (V)**	**Γ(cal)**	**Γ (obs)=V_{ac}/V_{dc}**	**% of error**
Bridge rectifier without filter					
Bridge rectifier with filter					

2) Observation On CRO/DSO For Rectified Output :

TYPE OF RECTIFIERCIRCUIT	**AMPLITUDE**	**TIME PERIOD**	**FREQUENCY**
Bridge rectifier without filter			
Bridge rectifier with filter			

VOLTAGE REGULATION:

% of voltage regulation= $[(V_{NL}-V_{FL})/V_{FL}]X100$

OBSERVATION TABLE:

V_{NL} (V)	**V_{FL} (V)**	**% OF REGULATION**

CONCLUSION:

SILIGURI INSTITUTE OF TECHNOLOGY

DEPT. OF E.C.E

Paper Code: EC 492 **Course Title : Analog Electronic Circuits Lab**

Experiment No.: 4 **Date:**

AIM: Design and setup the BJT common emitter amplifier using voltage divider bias and determine the gain-bandwidth product from its frequency response.

OBJECTIVES:

1. To design and setup a capacitor-coupled Common Emitter Amplifier with voltage divider bias according to a given specification.
2. To study the frequency response curve and determine the gain-bandwidth product.

THEORY:

Specification: Supply voltage (V_{CC}), minimum Voltage gain (A_V), Frequency response (lower cutoff (f_L) and upper cutoff frequency (f_H)), Signal source impedance (Z_S) and Load impedance (Z_L). Fig. 1 shows the circuit for a single-stage CE amplifier with voltage divider bias.

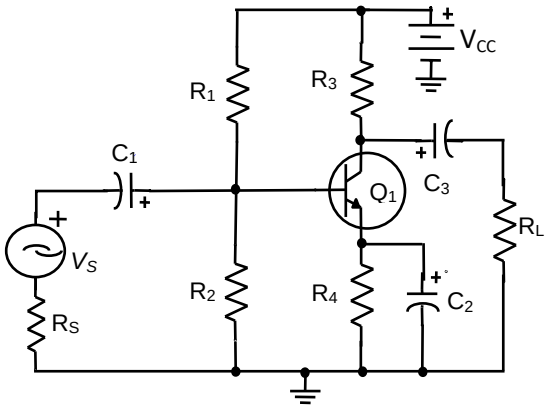


Figure 1(a): Single-stage CE amplifier circuit.

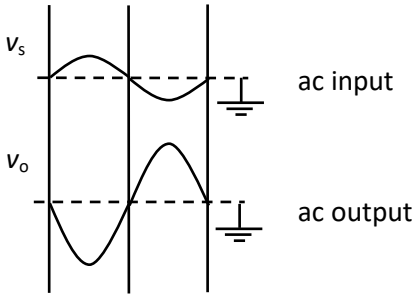


Figure 1(b): Voltage waveforms for a CE amplifier circuit.

Step 1: Selection of V_{CC}, I_C, R_C and R_E

Voltage gain, $A_V = \frac{-h_{fe}(R_C \,||R_L)}{h_{ie}}$

Therefore, A_V is proportional to R_CIIR$_L$. But large value of R_C will make the collector current I_C too small. A good minimum **I_C will be 1 mA** for small signal amplifier.

To ensure that the transistor operates linearly and to allow the collector voltage swing of ±1V, which actually adequate for a small signal amplifier, the collector-emitter voltage **V_{CE} should be around 3V**.

For good bias stability, emitter resistor voltage drop V_E should be much larger than base-emitter voltage V_{BE}. This is because,

$V_E = V_B - V_{BE}$, and when $V_E >> V_{BE}$, V_E will only be slightly affected by any variation in V_{BE} (due to temperature change or other effects). Consequently, I_E and I_C remain fairly stable at $I_C \approx I_E = V_E/R_E$.

With V_{CC}= 15V, we can choose V_E = 5V for a reasonable level of V_{CE} and V_{RC}.

Let us choose V_{CC} = 15V, V_{CE}= 3V, V_E= 5V, I_C = 1mA.

Then $V_{RC} = V_{CC} - V_{CE} - V_E = 15 - 3 - 5 = 7V$

$R_C = \frac{V_{RC}}{I_E} = \frac{7V}{1mA}$ = 7KΩ. We choose **R_C = 6.8 KΩ** as the standard value nearest to 7KΩ.

$R_E = \frac{V_E}{I_E} = \frac{5V}{1mA}$ = 5KΩ. We choose **R_E = 4.7 KΩ** as the standard value nearest to 5KΩ.

Step 2: Selection of Bias Resistors R_1 and R_2

The voltage divider current (I_2) may be selected as $I_C/10$ to achieve a good bias stability and reasonably high input resistance.

$R_2 = \frac{V_B}{I_2} = \frac{V_{BE} + V_E}{I_2/10} = \frac{(0.7 + 5)V}{1mA/10}$ = 57 KΩ. We choose **R_2= 56 KΩ** as the standard value nearest to 57KΩ.

$R_1 = \frac{V_{CC} - V_B}{I_2/10} = \frac{(15 - 5.7)V}{1mA/10}$ = 92KΩ. We choose **R_1= 100 KΩ** as the standard value nearest to 92 KΩ.

Step 2: Selection of Coupling Capacitors C1 and C_3

To minimize the effects of **C1 and C_3,** the reactance of each coupling capacitor is selected to be approximately equal to one-tenth of the impedance in series with it at the lowest operating frequency of the circuit (f_L).

$$X_{C1} = \frac{Z_i + r_s}{10} \text{ at } f_L$$

$$X_{C3} = \frac{Z_o + R_L}{10} \text{ at } f_L$$

Let the transistor 2N3904 is selected for this design.

From the datasheet of 2N3904 we have, h_{fe} = 70 (min) at I_C = 1 mA, V_{CE} = 1.0 V

$$r'e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1\text{ mA}} = 26\Omega$$

$$h_{ie} = (1 + h_{fe})r'e = (1+70) \text{ x } 26\ \Omega \approx 1.8\ k\Omega$$

Input impedance, $\mathbf{Z_i = R_1||R_2||}\boldsymbol{h_{ie}}$= 100kΩ||56kΩ||1.8 kΩ = 1.72 kΩ

$C_1 = \frac{1}{2\pi f_L(Z_i+r_s)/10}$ Signal source impedance, r_s = 50Ω = 0.05 KΩ

Let, f_L = 1000 H_Z

Therefore, $C_1 = \frac{1}{2\pi \text{ X } 1000 \text{ Hz X } (1.72\ k\Omega + 0.05K\Omega)/10} \approx 0.899\ \mu F$. We choose $\mathbf{C_1 = 1\ \mu F}$ as the standard value nearest to 0.899 μF.

As a rule of thumb, the value of R_L is selected as $10R_C$which is sufficient to keep the effect of R_L insignificant on the circuit voltage gain.

Hence, $\mathbf{R_L}$ **= 68 KΩ** is selected.

$C_3 = \frac{1}{2\pi f_L(R_C+R_L)/10} = \frac{1}{2\pi X 1000 Hz\ X(6.8\ k\Omega + 68\ K\Omega)/10} = 0.021\ \mu F$. We choose $\mathbf{C_3 = 22}$ nFas the standard value nearest to 0.021 μF.

Step 2: Selection of Bypass Capacitor C_2

$$X_{C2} = \frac{h_{ie}}{1+h_{fe}} \text{ at } f_L = \frac{1.8\ k\Omega}{1+70} = 25.35\Omega$$

$C_2 = \frac{1}{2\pi f_L X_{C2}} = \frac{1}{2\pi X 1000\text{ Hz X } 25.35\ \Omega} = 6.28\mu F$. We choose $\mathbf{C_2 = 10}$ μF as the standard value nearest to 6.28 μF.

The upper cut-off frequency (f_H) of circuit is set by simply connecting a capacitor (C_L) from the collector terminal to ground. Let us select f_H= 100 KHz.

$C_L = \frac{1}{2\pi f_H R_C} = \frac{1}{2\pi X 100kHz X 6.8K\Omega}$= 234 pF. We choose C_L = 220 pF as the standard value nearest to 234 pF.

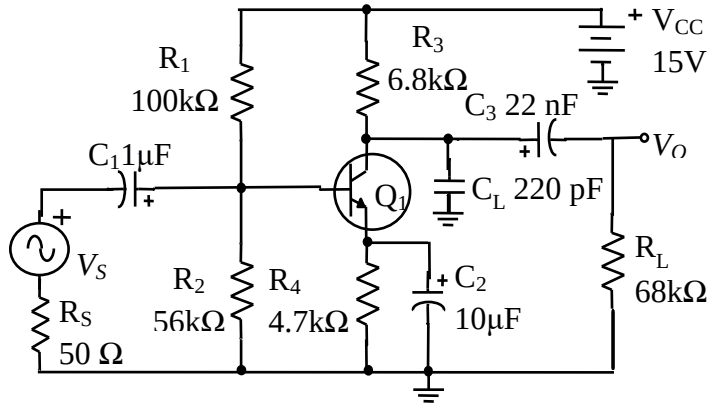


Figure 2: A designed capacitor-coupled CE amplifier.

Circuit Analysis

The h-parameter equivalent circuit is produced by replacing the supply voltage and all capacitors with short circuits and substituting device h-parameter model for the transistor as shown in figure 3.

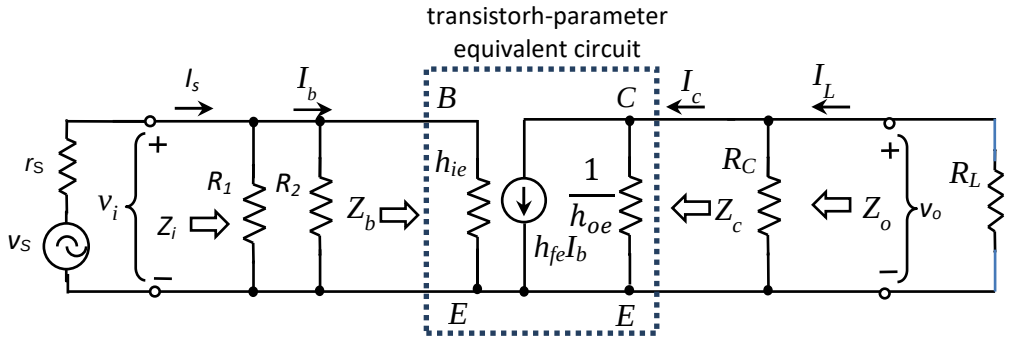


Figure 3: h-parameter equivalent circuit for a CE amplifier

Input impedance, $Z_i = R_1 || R_2 || h_{ie}$= 100kΩ||56kΩ||1.8 kΩ = 1.72 kΩ

Output impedance, $Z_o = R_c||(1/h_{oe})$

Since, $R_c << 1/h_{oe}$ $Z_o \approx R_c = 6.8\ k\Omega$

Voltage gain, $A_{v1} = \frac{-h_{fe}(R_c||R_L)}{h_{ie}}$

$= \frac{-70\times(6.8k\Omega\ \text{II}\ 68\ k\Omega)}{1.8\ k\Omega} \approx 240$

Design problem

Design a capacitor coupled CE amplifier with the following specification. Setup the circuit on a breadboard. Experimentally determine lower cut-off and higher cut-off frequency and bandwidth of circuit. Calculate the input and output impedance.

(a) V_{CC}= 15 V, (b) I_C = 1mA, (c) V_{CE} = 3V and (d) f_L= 1000Hz and f_H=100 kHz

Design Solution

The design of the capacitor coupled CE amplifier with the given specification is done in the theory part of this laboratory manual.

Procedure

a) Apply a fixed peak-to-peak amplitude sinusoidal signal within the range of 1 mV through 5mV to the input coupling capacitor C_1 from a signal generator's 50 Ω output terminal.
b) Vary the input signal frequency from 100 Hz to 900 Hz at the step of 100 Hz, from 1 kHz to 10 kHz at the step of 1 kHz, and from 20 kHz to 100 kHz at the step of 10 kHz, 200 kHz to 1MHz at the step of 100 kHz.
c) For each input signal frequency measure the peak-to-peak amplified output across the load resistor R_L with the help of a CRO and record in the observation table.
d) Draw the frequency response curve on a semi-log graph sheet and find out lower cut-off and upper cut-off frequencies and bandwidth.
e) Calculate the input and output impedance of the circuit.

Apparatus Required

Sl. No.	Devices/ Test equipment/ Power source	Value/ Make and model	Quantity

1.	NPN Transistor 2N3904	$V_{CE\ MAX}$ = 40V, $I_{C\ MAX}$ = 200mA, $h_{FE(min)}$ = 70	01
2.	Resistor (carbon film or metal film)	100 KΩ 68 KΩ 56 KΩ 6.8 KΩ 4.7 KΩ	01 01 01 01 01
3.	Capacitor	10 μF(Electrolytic) 1 μF (Electrolytic) 22 nF (Polypropylene) 220 pF (Ceramic Disc)	01 01 01 01
4.	Single Stand Wire (hook up wire)	24SWG	as required
5.	Bread Board	Wish	01
6.	Regulated DC Power	ELNOVA E-61 (+15V)	01
7.	Dual Channel Oscilloscope	Scientech/ GW Instek dc to 20 MHz	01
8.	Function Generator	GW Instek SFG-1013	01
9.	DMM	CIE-122	01

Observation Table

$\mathbf{V_{in}}$ = 5 mV (peak-to-peak)

Sl. No. of Obs.	**Frequency of input signal (Hz/ kHz)**	**$V_{O(p-p)}$ (V)**	**$A_V = \frac{V_O}{V_{in}}$**	**$A_v = 20log_{10}(\frac{V_O}{V_{in}})$ (dB)**	**f_L (Hz)**	**f_H (kHz)**	**3-dB Bandwidth (kHz)**
1.	100 Hz						
2.	200 Hz						
…	…						
…	…						
10	1 kHz						
11.	2 kHz						
…	…						
…	…						
20.	20 kHz						
21	30 kHz						
…	…						
…	…						
28.	100 kHz						
29.	200 kHz						
…	…						
…	…						
37	1000 kHz						

Calculation:

Discussion:

Conclusion:

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Paper Code: EC 492 **Course Title : Analog Electronic Circuits Lab**

Experiment No.: 5 **Date:**

AIM

Design a Class-AB Complementary Symmetry Power Amplifier with the given specifications. Find the

(1) Power output,
(2) Efficiency
(3) THD (total harmonic distortion)

THEORY

DESIGN PROBLEM

We have to design a Class AB complementary symmetry emitter follower power amplifier as shown in Figure 1(a) to deliver1 watt power to an 8 Ω load. The lower cut-off frequency (f_L) of the capacitor coupled amplifier to be chosen 1 KHz. We have to determine the required supply voltage (V_{CC}), and calculate resistor values for R_C, R_B, R_{E2}, and R_{E3}. Here we assume $h_{FE(min)} = 50$ for Q_2 and Q_3.

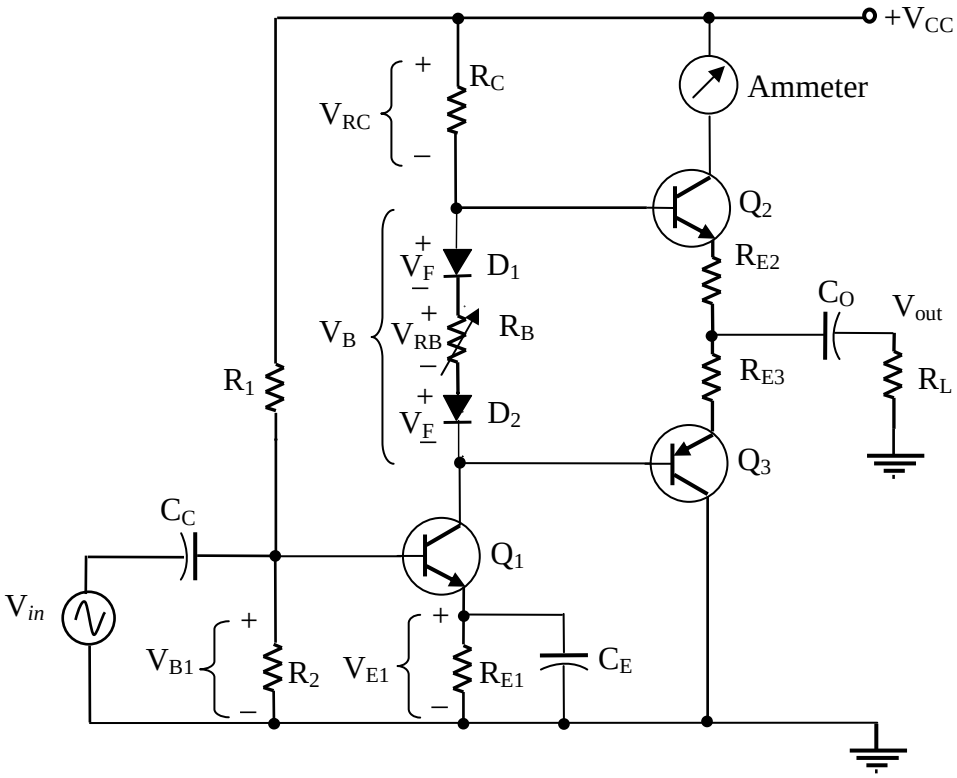

Fig 1(a): Class-AB Complementary Symmetry Power Amplifier

Solution

We know, peak voltage of the output waveform,

$$V_P = \sqrt{(2R_L P_O)} = \sqrt{(2 \times 8\Omega \times 1W)} = 4\text{V}$$

$$I_P = \frac{V_P}{R_L} = \frac{4V}{8\Omega} = 500 \text{ mA}$$

The voltage drops across R_{E2} and R_{E3} when the peak output current is flowing are typically selected as 5% to 10% of the peak output voltage. R_{E2} and R_{E3} are included to help stabilize the transistor quiescent current at a level that eliminates cross-over distortion in output waveform.

Hence,

$$R_{E2} = R_{E3} = 0.1\ R_L = 0.1 \times 8\ \Omega = 0.8\ \Omega \text{ (use 1 } \Omega \text{ standard value)}$$

Select , $I_{CQ2} = 0.1 I_P = 0.1 \times 500\ mA = 50$ mA

$$V_B = V_{BE2} + I_{CQ2}(R_{E2} + R_{E3}) + V_{BE3}$$

$$= 0.7\ \text{V} + 50\ \text{mA}\ (1\ \Omega + 1\ \Omega) + 0.7\ \text{V}$$

$$= 1.5\ \text{V}$$

When the output voltage is at its negative-going peak , the V_{CE1} should be 1 V minimum to ensure that Q_1 does not go into saturation. Also, V_{E1} should be typically 3 V. So, the minimum level of V_{C1} is typically 4 V. Similarly, when the output is at its positive-going peak, there must be an appropriate minimum voltage across resistor R_C. It is not acceptable to set a 1 V minimum for V_{RC}, because the current through R_C would be too small for the required peak base current to Q_2. It is best to select,

$$V_{RC(min)} = V_{C1(min)} = 4\ \text{V}$$

The minimum current through R_C ($I_{RC(min)}$) should be typically be selected 1 mA larger than the peak base current for the output transistors Q_2 and Q_3.

$$I_{B2(Max)} = \frac{I_P}{h_{FE2(min)}} = \frac{500\ mA}{50}$$

$$= 10\ \text{mA}$$

Select, $$I_{RC(min)} = I_{B2(max)} + 1\ \text{mA} = 10\ \text{mA} + 1\ \text{mA}$$

$$= 11\ \text{mA}$$

$$R_C = \frac{V_{RC(min)}}{I_{RC(min)}} = \frac{4\ \text{V}}{11\ \text{mA}}$$

$$= 360\ \Omega$$

We can find the V_{CC}, from the relation,

$$V_{CC} = 2\ (V_P + V_{RE2} + V_{BE2} + V_{RC(min)})$$

$$= 2(4 + 1\ \Omega \times 0.5\ A + 0.7\ V + 4\ V)$$

$$= 18.4\ \text{V} \qquad \text{(use 18 V)}$$

The voltage drop across the diodes and R_B should just bias Q_2 and Q_3 on for Class-AB operation. The current through R_B is the Q_1 quiescent current I_{CQ1}.

$$V_{RC(dc)} + V_{C1(dc)} = V_{CC} - V_B$$

Since, The dc voltage drop across R_C , $V_{RC(dc)}$ equals $V_{C1(dc)}$, we can write

$$V_{RC(dc)} = V_{C1(dc)} = 0.5(V_{CC} - V_B) = 0.5(18.4\,V - 1.5\,V)$$

Hence, $V_{RC(dc)} = 8.45$ V

$$I_{C1(dc)} = \frac{V_{RC(dc)}}{R_{C1}} = \frac{8.45\,V}{360\,\Omega}$$

$= 23$ mA

$$R_B = \frac{V_B - V_{D1} - V_{D2}}{I_{C1(dc)}} = \frac{1.5\,V - 0.7\,V - 0.7\,V}{23\,mA}$$

$= 4.35\ \Omega$ (use 20 Ω standard value variable resistor to allow for ± adjustment)

Resistors R_1, R_2 and R_{E1} are determined in the usual manner.

Since, $V_{E1} = 3\,V$, $R_{E1} = \frac{V_{E1}}{I_{C1(dc)}} = \frac{3\,V}{23\,mA}$

$= 130\ \Omega$ (use 120 Ω standard value resistor)

$$R_2 = \frac{V_{B1}}{0.1I_{C1(dc)}} = \frac{V_{BE1} + V_{E1}}{0.1I_{C1(dc)}} = \frac{0.7\,V + 3\,V}{2.3\,mA}$$

$= 1.6$ KΩ

$$R_1 = \frac{V_{CC} - V_{B1}}{0.1I_{C1(dc)}} = \frac{18\,V - 3.7\,V}{2.3\,mA}$$

$= 6.2$ KΩ

Design of coupling and Bypass capacitors, C_C, C_O and C_E

To minimize the effects of C_C and C_O, the reactance of each coupling capacitor is selected to be approximately one-tenth of the impedance in series with it at the lowest operating frequency for the circuit (f_L).

$$X_{Cc} = \frac{Z_i + r_s}{10} \text{ at } f_L$$

$$X_{Co} = \frac{Z_o + R_L}{10} \text{ at } f_L$$

Let the transistor SL100 for Q_1 is selected for this design.

From the datasheet of SL100 we have, $h_{fe} = 25$ (min) at $I_C = 10$ mA, $V_{CE} = 10$ V

$$r'e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{23\text{ mA}} = 1.13\ \Omega$$

$h_{ie} = (1 + h_{fe})r'e = (1+25) \times 1.13\ \Omega \approx 30\ \Omega$

Input impedance, $\mathbf{Z_i = R_1||R_2||}\boldsymbol{h_{ie}}$ = 6.2 kΩ||1.6 kΩ||30 Ω

= 29Ω

$C_C = \frac{1}{2\pi f_L(Z_i+r_s)/10}$ Signal source impedance, r_s = 50Ω

Let, Lower cut-off frequency, f_L = 1000 H_Z

Then, after solving we get C_C = 20 µF select 47 µF for C_C as nearest standard value.

$C_O \approx \frac{1}{2\pi f_L 0.1 R_L} = \frac{1}{2\pi \times 1000 \times 0.1 \times 8\,\Omega}$ = 199 µF

Select 220 µF for C_O as the nearest standard value.

We can write, $C_E \approx \frac{1}{2\pi f_L h_{ib1}} = \frac{1}{2\pi \times 1000 \times 1.13\Omega}$F

= 141 µF Select 220 µF for C_E as nearest standard value.

Completely designed Class AB Complementary Symmetry Power Amplifier is shown in Fig. 1(a).

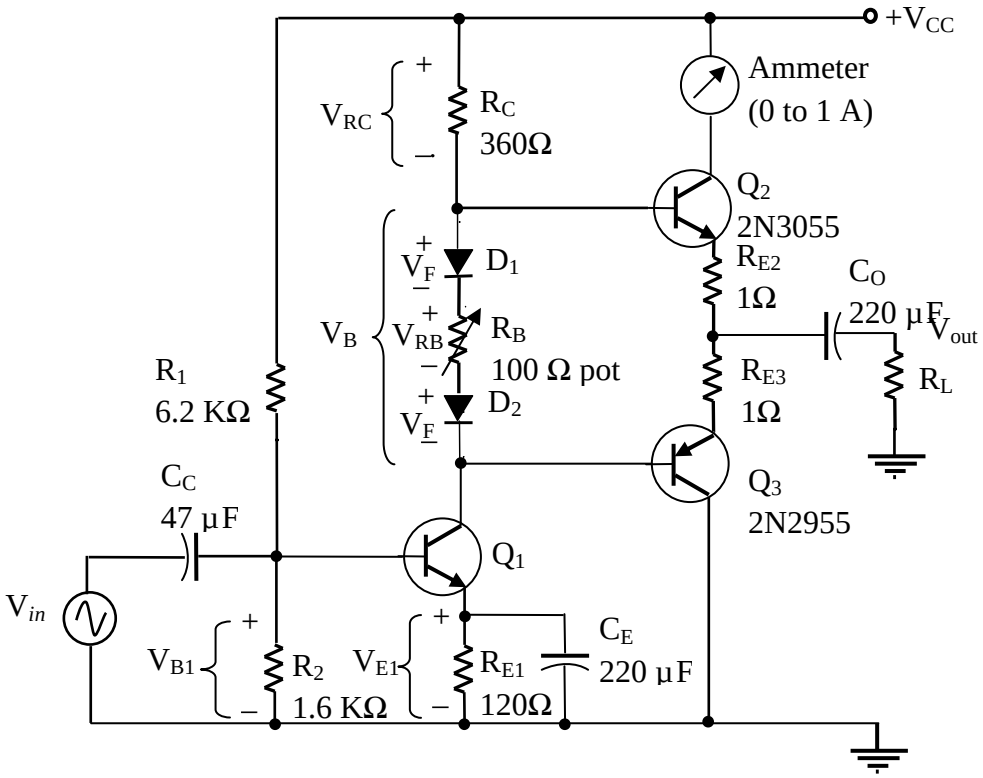

Fig 1(b): Class-AB Complementary Symmetry Power Amplifier

APPARATUS AND COMPONENTS REQUIRED:

Sl. No.	Devices/ Test equipment/ Power source	Value/ Make and model	Quantity
1.	Transistor SL100		01
2.	Transistor 2N3055		01
3.	Transistor 2N2955		01
4.	Diode 1N4007		02
5.	Resistor (carbon film or metal film)	1 Ω, 4 W 120 Ω,2W 1.6 kΩ 6.2 kΩ	02 01 01 01
6.	Capacitor	47 μF, 50 V(Electrolytic) 220 μF, 50 V (Electrolytic)	01 02
7.	Potentiometer	100 Ω	01
8.	Single Stand Wire (hook up wire)	24 SWG	1 m
9.	Bread Board	Wish	01
10.	Regulated DC Power	ELNOVA E-61 (0 to +30 V)	01
11.	Dual Channel Oscilloscope	Scientech/ GW Instek dc to 20 MHz	01
12.	Function Generator	GW Instek SFG-1013	01
13.	DMM	CIE-122	01

OBSERVATION TABLE:

Sl. No. of Obs.	Description of measurement	Calculated value	Observed value	% of error
1.	Vcc			
2.	V_{RE}			
3.	V_{RC}			
4.	V_{CEQ}			
5.	I_{CQ}			
6.	$v_{in(p-p)}$			
7.	P_o (max)			
8.	η			
9.	THD (total harmonic distortion)			

CONCLUSION:

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Paper Code: EC 492 **Course Title : Analog Electronic Circuits Lab**

Experiment No.: 6 **Date:**

AIM

To design and implement a transistor series voltage regulator with error amplifier and to determine line and load regulation characteristics.

THEORY

The function of an ideal voltage regulator is to maintain a constant voltage at its output terminals, no matter what current is drawn from it. The output voltage of a practical power supply changes with load current, generally dropping as load current increases. The power supply specifications include a full load current rating, which is the maximum current that can be drawn from the supply. The terminal voltage when full load current is drawn is called the full load voltage (V_{FL}). The no load voltage (V_{NL}) is the terminal voltage when zero current is drawn from the supply, that is, the open circuit terminal voltage.

One measure of power supply performance, in terms of how well the power supply is able to maintain a constant voltage between no load and full load conditions, is called its percentage voltage regulation.

An unregulated power supply has poor regulation, i.e., output voltage changes with load variations. If a power supply has poor regulation it possesses high internal impedance. A simple emitter follower regulator is shown in Fig.1. It is also called a series regulator since the control element (transistor) is in series with the load. It is also called as the series-pass transistor because it conducts or passes all the load current through the regulator. It is usually a power transistor. The zener diode provides the voltage reference, and the base to emitter voltage of the transistor is the control voltage.

The value of R_S must be sufficiently small, to keep the zener in its reverse breakdown region. Writing Kirchhoff's voltage law to the output circuit,

$$V_O + V_{BE} - V_Z = 0$$

$$\text{i.e.,} \quad V_{BE} = V_Z - V_O$$

$$\text{also,} \quad V_O = V_Z - V_{BE}$$

If V_Z is perfectly constant, the above equation is valid at all times, and any change in V_O must cause change in V_{BE}, in order to maintain equality.

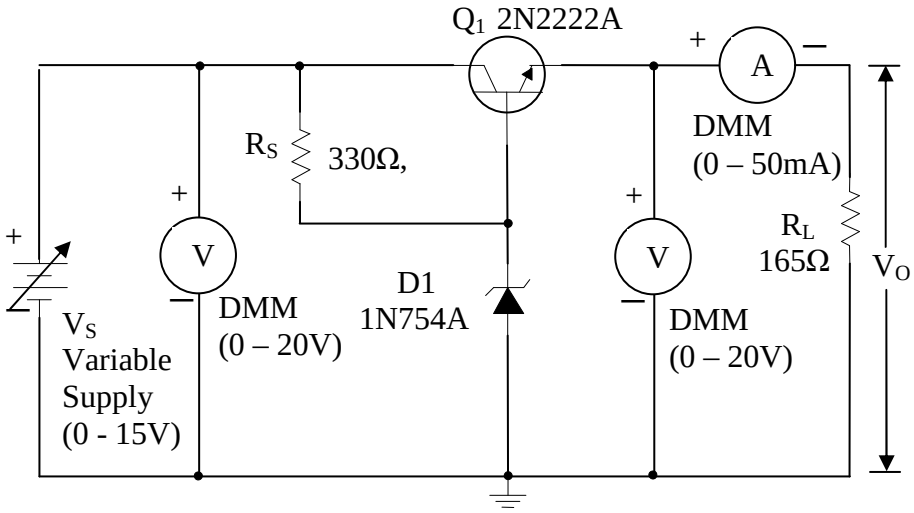


Fig. 1 Circuit diagram of a simple series voltage regulator

When load current demand is increased by decreasing R_L, V_O tends to decrease. From the above equation, it is seen that as V_Z is fixed, decrease in V_O increases in V_{BE}. This will increase the forward bias of the transistor, thereby increasing level of conduction. Thus, the output current is increased to keep $I_L R_L$ a constant. The reverse process occurs when R_L is increased. Thus, the above circuit keeps the output voltage constant, even if the load varies widely.

Series regulator using an error amplifier

A series regulator using an error amplifier as shown in fig.2 improves the line and load regulation of the circuit. In comparison to the simple regulator circuit in fig.1, where the zener voltage is greater than the output voltage, this amplifier makes it possible to have an output voltage greater than the zener voltage.

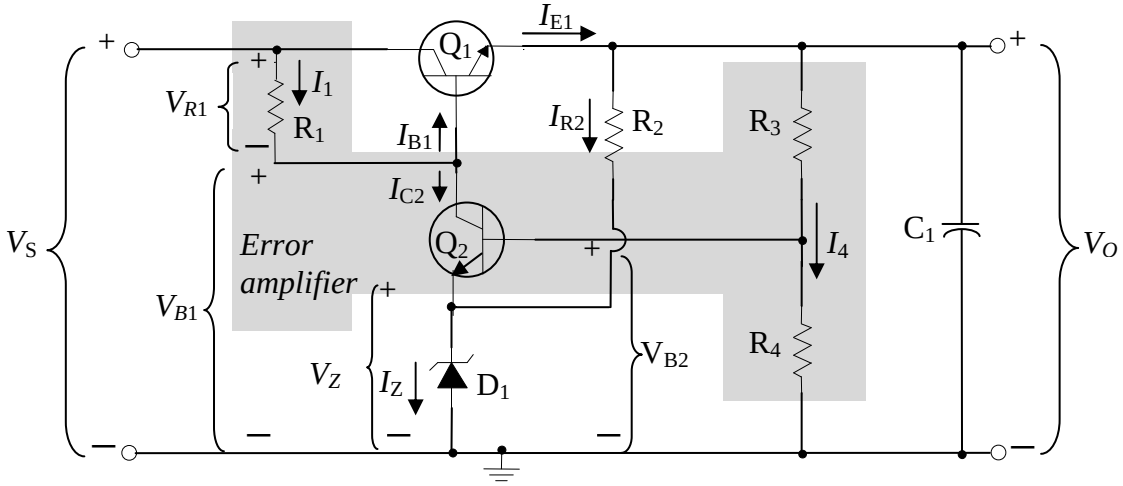


Fig. 2: Series voltage regulator circuit with an error amplifier

The Zener diode D_1 with resistor R_2 plays the role of a reference source. Transistor Q_2 along with its associated components resistor R_1, R_3 and R_4 constitute the error amplifier which controls emitter current I_{E1} of the series pass transistor Q_1. The output is divided by resistors

R_3 and R_4 and compared to Zener diode voltage level V_Z.

When the output voltage V_O changes, the change is amplified by transistor Q_2 and fed back to the base of Q_1 to correct the output voltage level. Suppose the regulator is designed for V_O 12 V and the DC supply V_S = 18 V. In this case the suitable Zener diode should be selected for V_Z = 6 V. For this level of V_Z the base voltage of Q_2 can be found as

$$V_{B2} = V_Z + V_{BE2} = 6.7 \text{ V}.$$

So resistors R_3 and R_4 are selected to give V_{B2} = 6.7 V and V_O = 12 V. The voltage at the base of Q_1 is

$$V_{B1} = V_O + V_{BE1} = 12.7 \text{ V}.$$

Also, $V_{R1} = V_S - V_{B1} = 18 - 12.7 = 5.3$ V.

The current through R_1 is mostly the collector current of Q_2.

Let us see how this regulator works. Assume that the output voltage drops slightly for some reason. When V_O decreases, V_{B2} decreases. Since the emitter voltage of Q_2 is tied at V_Z, any decrease in V_{B2} appears across at the base-emitter of Q_2. A reduction in V_{BE2} causes I_{C2} to be reduced. When I_{C2} falls, V_{R1} is reduced and the voltage at the base of Q_1 rises (since, $V_{B1} = V_S - V_{R1}$) causing the output voltage to increase. Thus, a decrease in the output voltage produces a feedback effect which causes the output voltage to increase back toward its normal level. Similarly, a rise in V_O above its normal level produces a feedback effect that pushes V_O down again toward its normal level. C_1 is a large value capacitor, usually 50 μF to 100 μF, which is connected at the output to suppress any tendency of the regulator to oscillate.

The error amplifier in the regulator improves all aspects of the circuit performance by an amount directly related to the amplifier voltage gain (A_V). When V_S changes by ΔV_S, the output voltage is

$$\Delta V_o = \frac{\Delta V_S}{A_v}$$

REGULATOR DESIGN

Design problem:

Design a voltage regulator circuit as shown in fig. 2 to produce regulated V_O = 9V and $I_{L(max)}$ = 40 mA. The supply voltage range is 12 to 15 V DC.

Solution:

Specifications:

Output Voltage, V_O = 9 V

Output Current, $I_{L(MAX)}$ = 40 mA

Input Voltage, V_i = 12 to 15 V DC

Select $V_Z \approx 0.75\ V_O = 0.75 \text{ X } 9 \text{ V}$

$= 6.75$ V

For Zener diode D_1 we can use 1N754, with V_Z = 6.8 V (I_{ZT} = 20 mA, I_{ZM} = 60 mA, P_D = 400

mW)

For minimum D_1 current, choose

I_{R2} = 20 mA

$$R_2 = \frac{V_O - V_Z}{I_{R2}} = \frac{9\,V - 6.8\,V}{20\,mA}$$

= 110 Ω (wattage of R_2 is $(20\text{ mA})^2 \times 110\ \Omega = 0.044$ W, choose 1/2W)

$I_{E1(max)} \approx I_{L(max)} + I_{R2}$ = 40 mA + 20 mA

= 60 mA

$$R_L = \frac{V_O}{I_L} = \frac{9\,V}{40\,mA}$$

= 225 Ω We choose 220 Ω, nearest standard value.

Specifications of Q_1:

$V_{CE1(max)} \approx V_S$ = 15 V

$I_{C1(max)} \approx I_{E1(max)}$ = 60 mA

$P_{D(max)} = (V_S - V_O) \times I_{E1(max)} = (15\text{ V} - 9\text{ V}) \times 60$ mA

= 360 mW

Assuming $h_{FE1(min)}$ = 100 We choose 2N2222A for Q_1

$$I_{B1(max)} = \frac{I_{E1(max)}}{h_{FE1(min)}} = \frac{60\,mA}{100}$$

= 0.6 mA

$I_{C2} > I_{B1(max)}$

Select I_{C2} = 2.5 mA

$$R_1 = \frac{V_S - V_{B1}}{I_{C2} + I_{B1}} = \frac{15\,V - (9\,V + 0.7)}{2.5\,mA + 0.6\,mA}$$

= 1.71 KΩ (use 1.8 KΩ standard value)

$I_Z = I_{E2} + I_{R2}$ = 2.5mA + 20 mA

= 22.5 mA

$I_4 >> I_{B1}$

Select I_4 = 1 mA

$$R_4 = \frac{V_Z + V_{BE2}}{I_4} = \frac{6.8\,V + 0.7\,V}{1\,mA}$$

= 7.5 KΩ

$$R_3 = \frac{V_O - V_{R4}}{I_4} = \frac{9\,V - 7.5\,V}{1\,mA}$$

= 1.5 KΩ

Select Q_2 a NPN transistor of small signal amplifier viz. BC548B

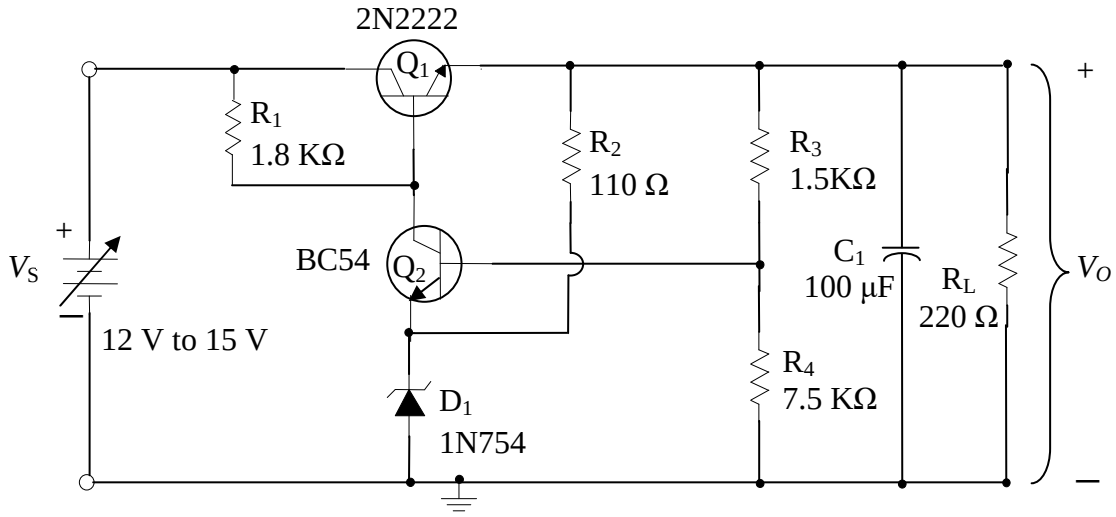


Fig. 3: Series voltage regulator circuit with an error amplifier (designed)

PROCEDURE

Load regulation

1. The circuit is wired as per the circuit diagram shown in fig. 2.
2. Keep the input voltage constant at $V_{i(min)}$, i.e. 12 V.
3. Vary the load resistance. Note I_L and V_O for each setting of R_L. Ensure that V_i remains same throughout.
4. Draw a plot between I_L and V_O.

Line Regulation

Percentage of line regulation is another measure of the ability of a power supply to maintain a constant output voltage. In this case, it is a measure of how sensitive the output is to the changes in input or line voltage rather than to the changes in load. The specification is usually expressed as the percentage of change in output voltage that occurs per volt change in input voltage, with the load R_L assumed constant.

1. The circuit diagram is wired as per the circuit diagram shown in fig. 1.
2. Keep the load resistance R_L a constant.
3. Vary the input voltage between the limits for which the regulator is designed (12 to 15V).
4. Note the load voltage V_O for each setting of V_{in}.
5. Draw a graph between V_{in} (X axis) and V_L (Y axis).

OBSERVATIONS

(a) Load Regulation

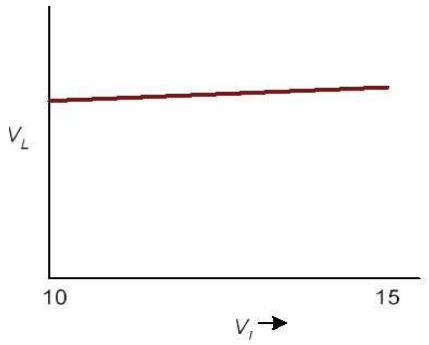
Load Resistance	Output	Load Current

(R_L)	Voltage V_O (V)	I_L (mA)

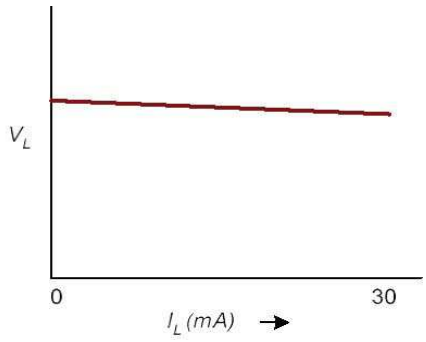
(b) Line Regulation

Line input Voltage V_i (V)	Output Voltage V_O (V)

Expected Output Plots



Line Regulation



Load Regulation

Result

Line regulation and load regulation curves are plotted.

Conclusion

SILIGURI INSTITUTE OF TECHNOLOGY

DEPT. OF E.C.E

Paper Code: EC 492 **Course Title : Analog Electronic Circuits Lab**

Experiment No.: 7 **Date:**

AIM

Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.

(a) Hartley Oscillator and (b) Colpitts Oscillator

THEORY

LC oscillators are generally used as RF oscillators since they are generally used to create high frequency oscillations. In Hartley and Colpitts oscillator an LC tank circuit is used for selection of frequency of oscillation. A voltage divider biased common emitter amplifier is used as amplifier. The amplifier and tank circuit together provides a phase shift of 360 degrees to satisfy Barkhausen criterion.

HARTLEY OSCILLATOR

COMPONENTS REQUIRED:

Sr. No.	Components	Range/Rating	Quantity
1.	Transistor	SL-100	1
2.	Resistance	270 Ω, 1/4 W	1
3.	Resistance	1 KΩ, 1/4 W	1
4.	Resistance	15 KΩ, 1/4 W	1
5.	Resistance	2.7 KΩ, 1/4 W	1
6.	Capacitor	0.47 µF	2
	Capacitor	47 µF	1
7.	Capacitor	470 pF	1
8.	Inductor	100 µH	2
9.	Potentiometer	1 KΩ	1
10.	Bread Board		1
11.	Hookup wire	25 SWG	

APPARATUS REQUIRED:

Sr. No.	Name of the Apparatus	Quantity	Range/Rating	Make
1.	Variable DC Regulated Power Supply	1	0 – 15 V	ELNOVA
2.	Digital Multimeter	1		
3.	CRO or DSO	1	20 MHz	
4.	Single Strand Connecting Wire	50 cm	24 SWG or 25 SWG	

Design:

BJT-Amplifier design is same as given in Common Emitter Amplifier**.**

Tank Circuit Design:

Oscillator Frequency $f = f_o$

$$Leq = L1 + L2$$

Assume f_o = 500 KHz, with $L1 = L2$ =100μH,

We get, $Leq = L1 + L2$ = 200μH

We know, $$f_o = \frac{1}{2\pi\sqrt{(LC)}}$$

Hence, $Leq \times C = 1/(2\pi f_o)^2$

This gives C = $\{1/(2\pi f_o)^2\}/\{Leq\}$

= $\{1/(2\pi \times 500\ \text{KHz})^2\}/200\ \mu H$

= 507 pF Choose 470 pF as standard value

For this capacitance value we get $\boldsymbol{f_o}$ **= 519 KHz**

CIRCUIT DIAGRAM:

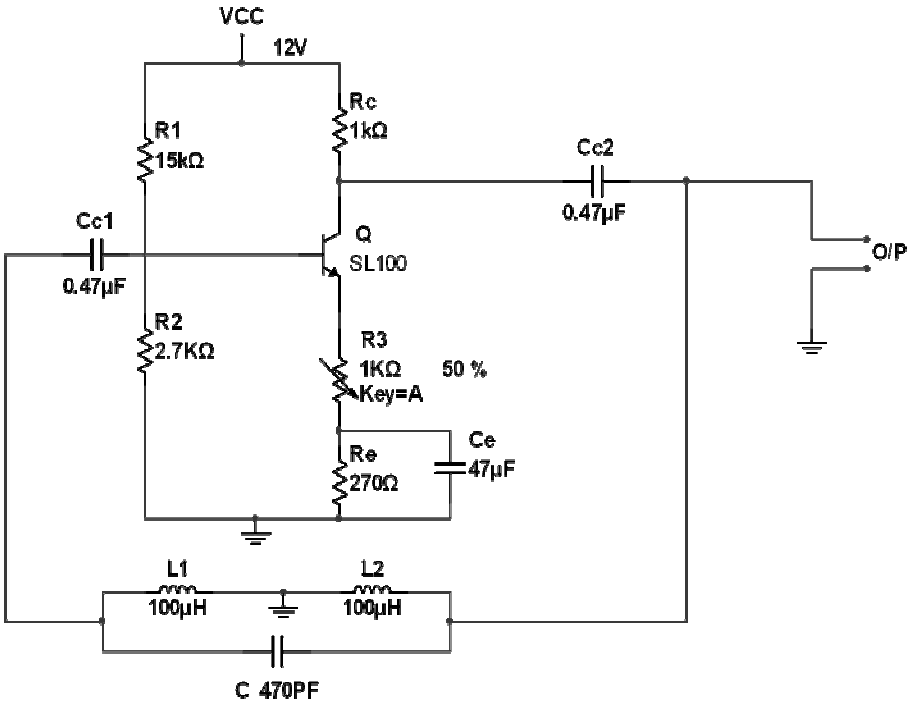


Fig1: Hartley Oscillator (designed)

Procedure:

1. Switch on the Power Supply and check the DC conditions by removing the coupling capacitor CC_1 or CC_2.
2. Connect the coupling capacitors and obtain an output wave form on the CRO .If the o/p is distorted vary 1 KΩ Potentiometer (R3) to get perfect SINE wave.
3. Measure the period of oscillation and calculate the frequency of oscillation.
4. Compare the measured frequency with re-computed theoretical value for the component values connected.

Observation:

Parameter	VRC	VCE	VE	ICQ = VRC / RC	VBE	VB
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V	4.8V
Practical						

Result: The frequency of oscillation is **…….**

COLPITTS OSCILLATOR

Components and equipments required:

Sr. No.	Components	Range/Rating	Quantity
1.	Transistor	BC107B	1
2.	Resistance	270 Ω, 1/4 W	1
3.	Resistance	1 KΩ, 1/4 W	1
4.	Resistance	15 KΩ, 1/4 W	1
5.	Resistance	2.7 KΩ, 1/4 W	1
6.	Capacitor	0.47 µF	2
7.	Capacitor	0.2 µF	1
8.	Capacitor	0.02 pF	2
9.	Inductor	15 µH	2
10.	Potentiometer	1 KΩ	1
11.	Bread Board		1
12.	Hookup wire	25 SWG	1m

Design:

In the Colpitts Oscillator shown in Fig. 2 capacitor C_3 and C_4 along with L_1 makes the LC tuned circuit. A voltage divider biased common emitter amplifier is used as amplifier. The amplifier and tank circuit together provides a phase shift of 360 degree to satisfy Barkhausen criterion.

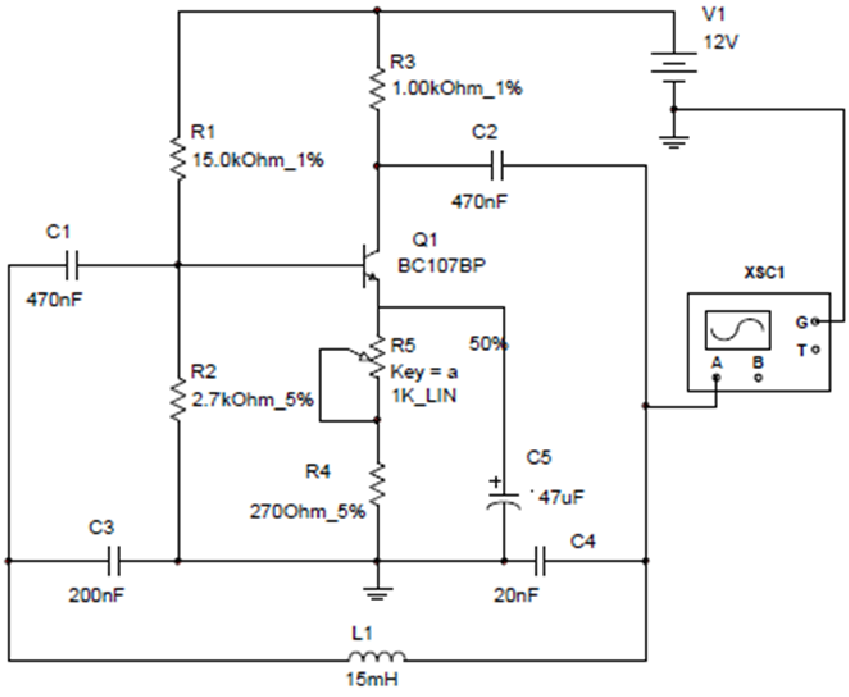


Fig. 2 Colpitts Oscillator

Design:

BJT-Amplifier design is same as given in Common Emitter amplifier**.**

Tank Circuit Design:

Assume f_o = 10 KHz, with C_3 = 200 nF, C_4 = 20 nF and frequency of oscillation 10KHz we have to find value of inductor L_1.

We know, $$f_o = \frac{1}{2\pi}\left(\sqrt{\left(\frac{C_3 + C_4}{L_1 C_3 C_4}\right)}\right)$$

Hence, $$L_1 = \frac{C_1 + C_3}{4\pi^2 f_o^2 C_1 C_2}$$

After solving, inductor value we get L_1 = 13.932 mH

Voltage gain to produce oscillation is $A_V > C_3/ C_4$

Procedure:

1. Switch on the Power Supply and check the DC conditions by removing the coupling capacitor CC_1 orCC_2.
2. Connect the coupling capacitors and obtain an output waveform on the CRO. If the o/p is distorted adjust 1-KΩ Potentiometer (R5) to get perfect SINE wave.
3. Measure the period of oscillation and calculate the frequency of oscillation.
4. Compare the measured frequency with re-computed theoretical value for the component values connected.

Observation:

Parameter	VRC	VCE	VE	ICQ = VRC / RC	VBE	VB
Assumed	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V
Practical						

Result: The frequency of oscillation is **…..**

SILIGURI INSTITUTE OF TECHNOLOGY

DEPT. OF E.C.E

Paper Code: EC 492 **Course Title : Analog Electronic Circuits Lab**

Experiment No.: 8 **Date:**

AIM: Plot the transfer and drain characteristics of n-channel MOSFET and calculate the following parameters.

1. Drain resistance (r_D),
2. Transconductance (g_m) and
3. Amplification factor (μ)

Theory:

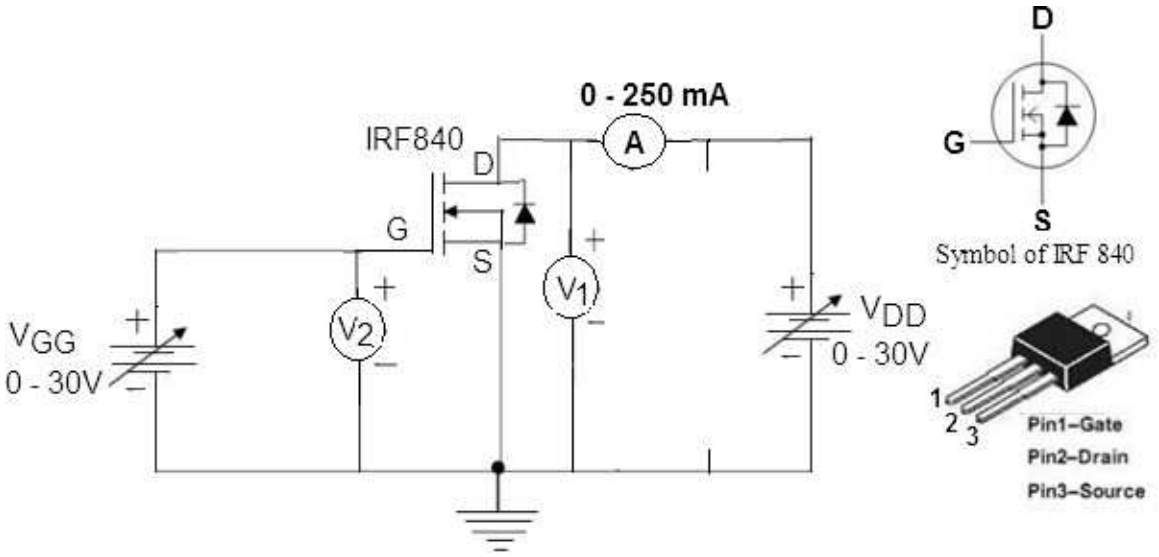
In a MOSFET, current flows from the drain terminal to the source terminal through a semiconductor channel. The resistance of the channel, and therefore its ability to conduct current, is controlled by a voltage applied to a third terminal denoted as the gate. MOSFETs can be either an n-channel type or a p-channel type. In an n-channel MOSFET a positive voltage is applied to the drain terminal for operation while in a p-channel MOSFET a negative voltage is applied to the drain terminal for operation. An n-channel and p-channel type MOSFET may be one of two modes; enhancement mode or depletion mode. The enhancement mode MOSFET is normally "OFF" (in cutoff and conducting no current) when no voltage is applied to the gate and is "ON" (in saturation and conducting current) when a voltage greater than the gate-to-source threshold is applied to the gate. The depletion mode MOSFET is normally "ON" (in saturation and conducting current) when no voltage is applied to the gate and is "OFF" (in cutoff and not conducting current) when a voltage more negative than the gate-to-source threshold is applied to the gate.

Components and equipment required:

Sl. No.	Components/Test Equipment	Quantity
1.	MOSFET IRF840	01
2.	Resistor-100 Ω	01

3.	Bread board	01
4.	1/24 SWG single strand wire	1m
5.	Regulated Power supply 0 to +30 V	02
6.	Digital Multimeter	03

Circuit setup diagram:



Procedure:

Follow the below mentioned steps to obtain the **Drain Characteristics**

1. Set up the connections as indicated in the figure.
2. Keep both V_{GG} and V_{DD} at zero position.
3. By varying V_{GG} set V_{GS} to some value (slightly greater than the Threshold voltage determined from the transfer characteristics) Say +3.0V
4. Increase V_{DS} by varying V_{DD} gradually and note down the corresponding meter readings as shown in the table.
5. Repeat the steps 3 and 4 for V_{GS} =+3.2V and V_{GS} = +3.4V
6. Plot the graph of I_D vs. V_{DS}

Observation Table: Drain Characteristics

V_{GS} = 3.0 V		V_{GS} = 3.2 V		V_{GS} = 3.4 V	
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)
0.0		0.0		0.0	

0.2		0.2		0.2	
0.4		0.4		0.4	
0.6		0.6		0.6	
0.8		0.8		0.8	
1.0		1.0		1.0	
1.5		1.5		1.5	
2.0		2.0		2.0	
3.0		3.0		3.0	
4.0		4.0		4.0	
5.0		5.0		5.0	
10.0		10.0		10.0	
12.0		12.0		12.0	
15.0		15.0		15.0	
18.0		18.0		18.0	
20.0		20.0		20.0	

Procedure:

Follow the below mentioned steps to obtain the Transfer Characteristics

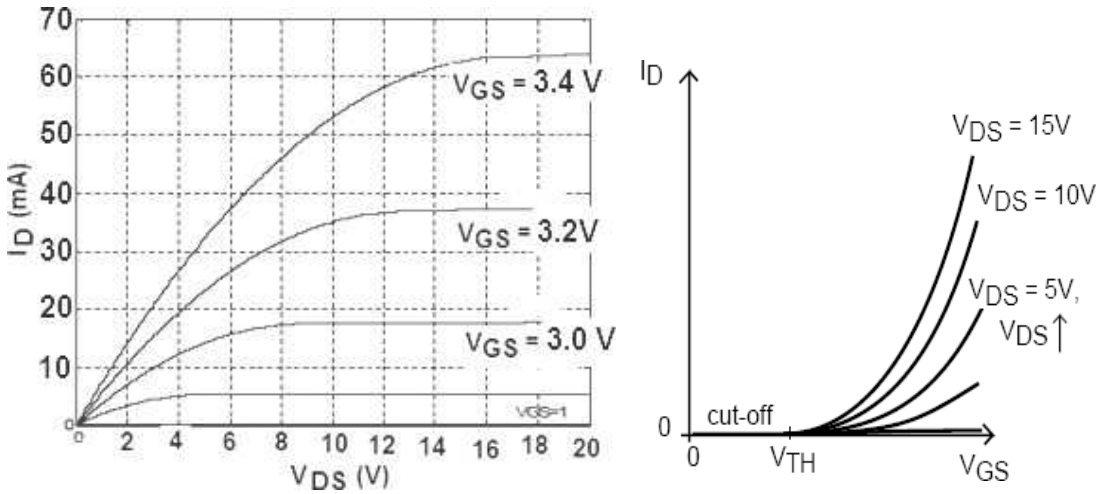
1. Set up the connections as indicated in the figure.
2. Keep both V_{GG} and V_{DD} at zero position.
3. Vary the V_{DD} and set V_{DS} = 1V.
4. Increase V_{GS} by varying V_{GG} gradually and note down the corresponding meter readings as shown in the table.
5. Note down the minimum value of V_{GS} for which drain current starts flowing and record V_{TH} =
6. Repeat for V_{DS} = 5 V, 10 V, and 15 V.
7. Plot the graph of I_D vs. V_{GS}

Observation Table: Transfer Characteristics

V_{DS} = 1.0 V		V_{DS} = 5.0 V		V_{DS} = 10.0 V		V_{DS} = 15.0 V	
V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)
1.0		1.0		1.0		1.0	
2.0		2.0		2.0		2.0	
2.9		2.9		2.9		2.9	
3.0		3.0		3.0		3.0	
3.1		3.1		3.1		3.1	
3.2		3.2		3.2		3.2	

3.3		3.3		3.3		3.3	
3.4		3.4		3.4		3.4	
3.5		3.5		3.5		3.5	
3.8		3.8		3.8		3.8	
4.0		4.0		4.0		4.0	
4.2		4.2		4.2		4.2	
4.5		4.5		4.5		4.5	

Expected graphs:



(a) Drain Characteristics **(b) Transfer Characteristics**

From the curves determine:

Transconductance gm $= \Delta I_D / \Delta V_{GS}$ mho

Drain Resistance $r_D = \Delta V_{DS} / \Delta I_D \Delta$

Amplification factor $\mu = g_m \times r_D$

Conclusion:

SILIGURI INSTITUTE OF TECHNOLOGY

DEPT. OF E.C.E

Paper Code: EC 492 **Course Title : Analog Electronic Circuits Lab**

Experiment No.: 9 **Date:**

AIM

This experiment will investigate the characteristics of the common-source and common-drain amplifier.

Material and Equipment

NTE 312 N Channel JFET.
Resistors: 2 k (2), 3.9 KΩ, 10 KΩ (2), 100 KΩ, 200 KΩ, 1 MΩ. Capacitors: 100 µF, 47µF, 1µF.

Theory

In this lab, two JFET amplifier configurations will be investigated; the common-source, and the common-drain amplifier.

The basic common-source circuit is shown in Fig. 1. In comparison to the BJT common-emitter amplifier, the FET amplifier has much higher input impedance, but a lower voltage gain.

The voltage gain of the circuit can be expressed as

$$A_v = -g_m R_D$$

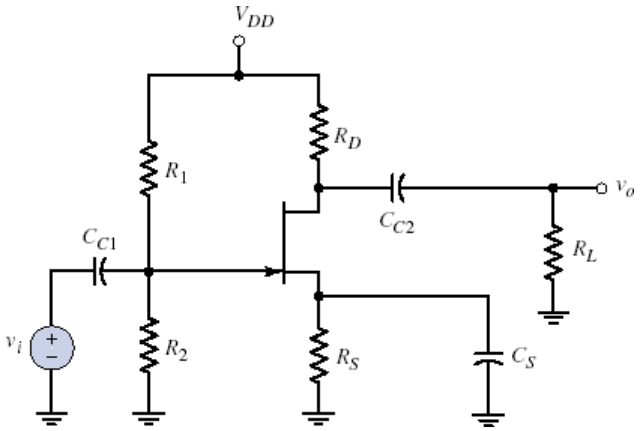


Figure 1: Common-Source Amplifier

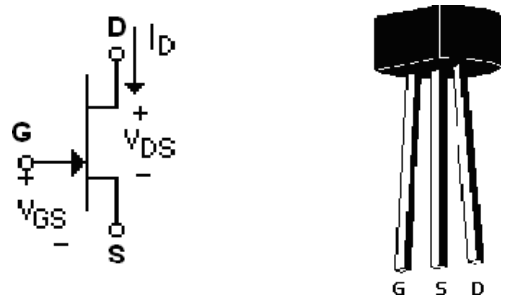


Figure 2: The Junction Field Effect Transistor(NTE 312)

Figure 2 shows the transistor terminals for your reference..

The common-drain (CD) amplifier is shown in figure 3. The common-drain configuration is often called a source follower as the voltage gain is nearly unity. The common drain FET amplifier is similar to the common collector configuration of the bipolar junction transistor.

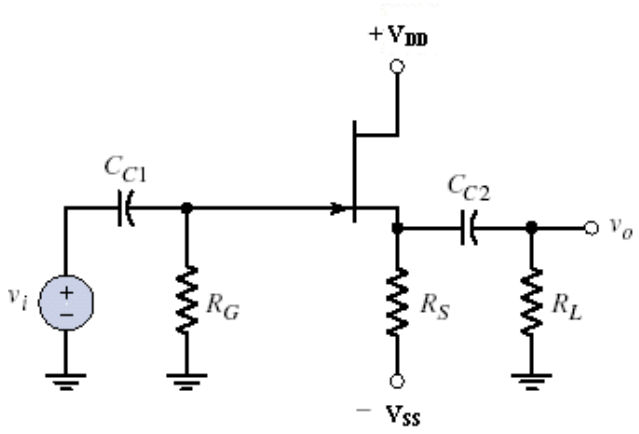


Figure 3: Common-Drain Amplifier

Procedure

1) Common-Source Amplifier
   a) Connect the circuit as shown in figure9-1.
   b) Use C_{c1} = 1µF, C_{c2} = 47µF, C_s=100 µF, R_L =3.9 k, R_S=R_D=2 k, R_1 = 200 KΩ , R_2=100 KΩ, V_{DD} = 12 V.
   c) Apply a sinusoidal signal with frequency 1 KHz, amplitude 1Vp-p, and supply voltages at10 V.
   d) Observe the output.
   e) Capture both input and output waveforms.
   f) Calculate the voltage gain.
   g) Measure the operating point.

1) Common-Drain Amplifier

a) Connect the circuit as shown in figure9-2.

b) Use R_G = 1 M Ω, R_S = R_L = 10 K Ω, supply V_{DD} = 10 V and V_{SS}= - 10 V.

c) Apply a sinusoidal signal with frequency 1 KHz, amplitude 2Vp-p.

d) Observe the output.

e) Capture both input and output waveforms.

f) Calculate the voltage gain.

g) Measure the operating point.

Questions for the Lab Report

Compare BJT and JFET (in terms of characteristics, applications, merits and demerits but not constructional details)

SILGURI INSTITUTE OF TECHNOLOGY

LABORATORY MANUAL OF COMPUTER ORGANIZATION

CODE: CS393 CONTACTS: 3 CREDITS: 2

1. Familiarity with IC chips, e.g.
   a) Multiplexer
   b) Decoder
   c) Encoder
   d) Comparator

Truth Table Verification and clarification from data –book

2. Design an Adder/Subtract or composite unit.
3. Design a BCD Adder.
4. Use a multiplexer unit to design a composite ALU
5. Use ALU chip for multibit.
6. Implement read /write operation using RAM IC.
7. a) Cascade two RAM ICs for vertical expansion.
   b) Cascade two RAM IC for horizontal expansion.

EXPERIMENT NO. : 01.(a)

NAME OF THE EXPERIMENT : Familiarity with IC-Chips, a) Multiplexer.
Truth Table verification and clarification from Data-Book.

COMPONENTS REQUIRED : IC – 74153
IC – 74150

THEORY :

Multiplex means many into one. Multiplexer is transmitting a large number of information unit over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of particular input line is controlled by set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combination determine which input is selected. A multiplexer is also called a "Data Selector", since it selects one of many inputs and steers the binary information to the output li

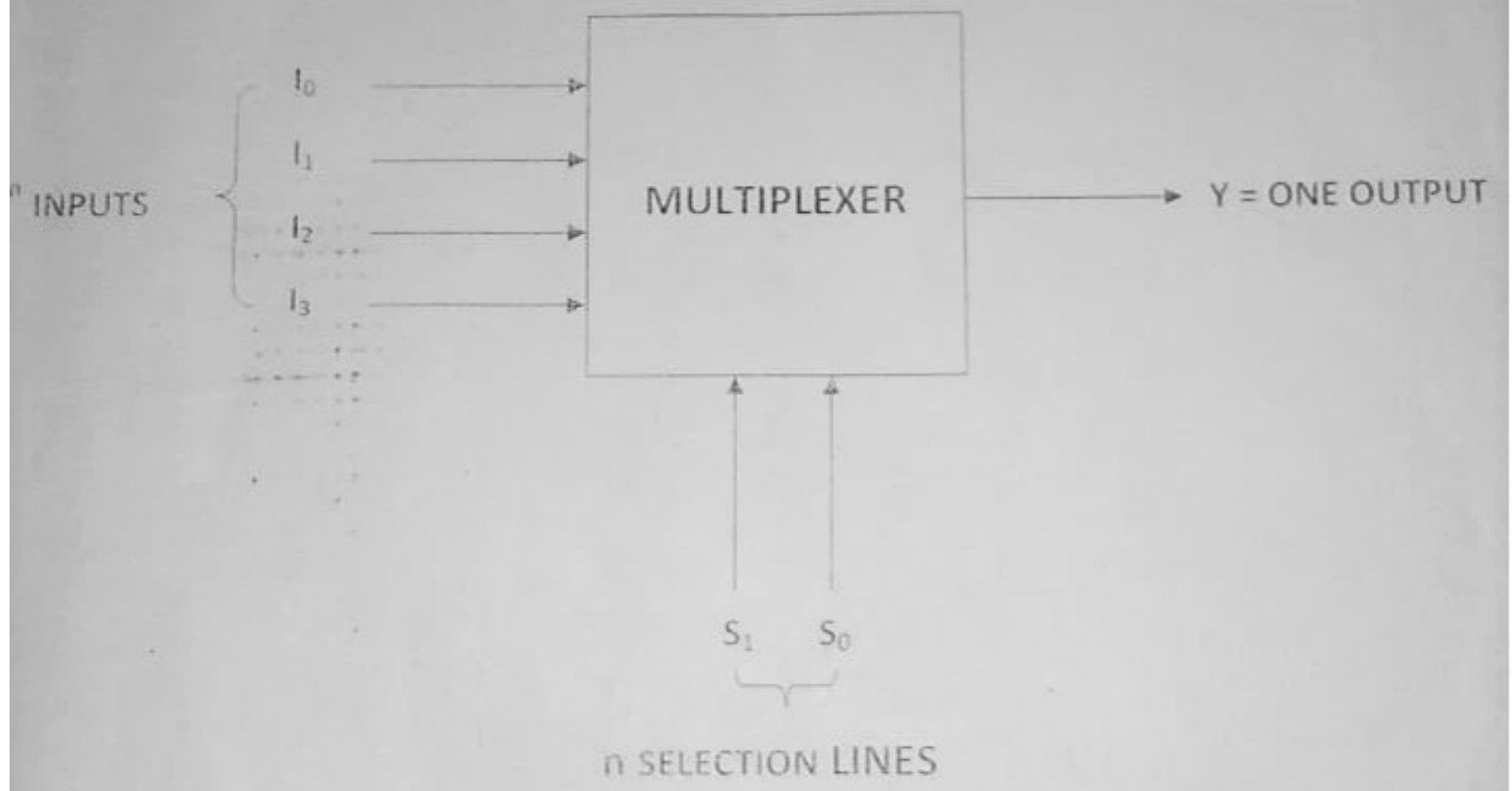
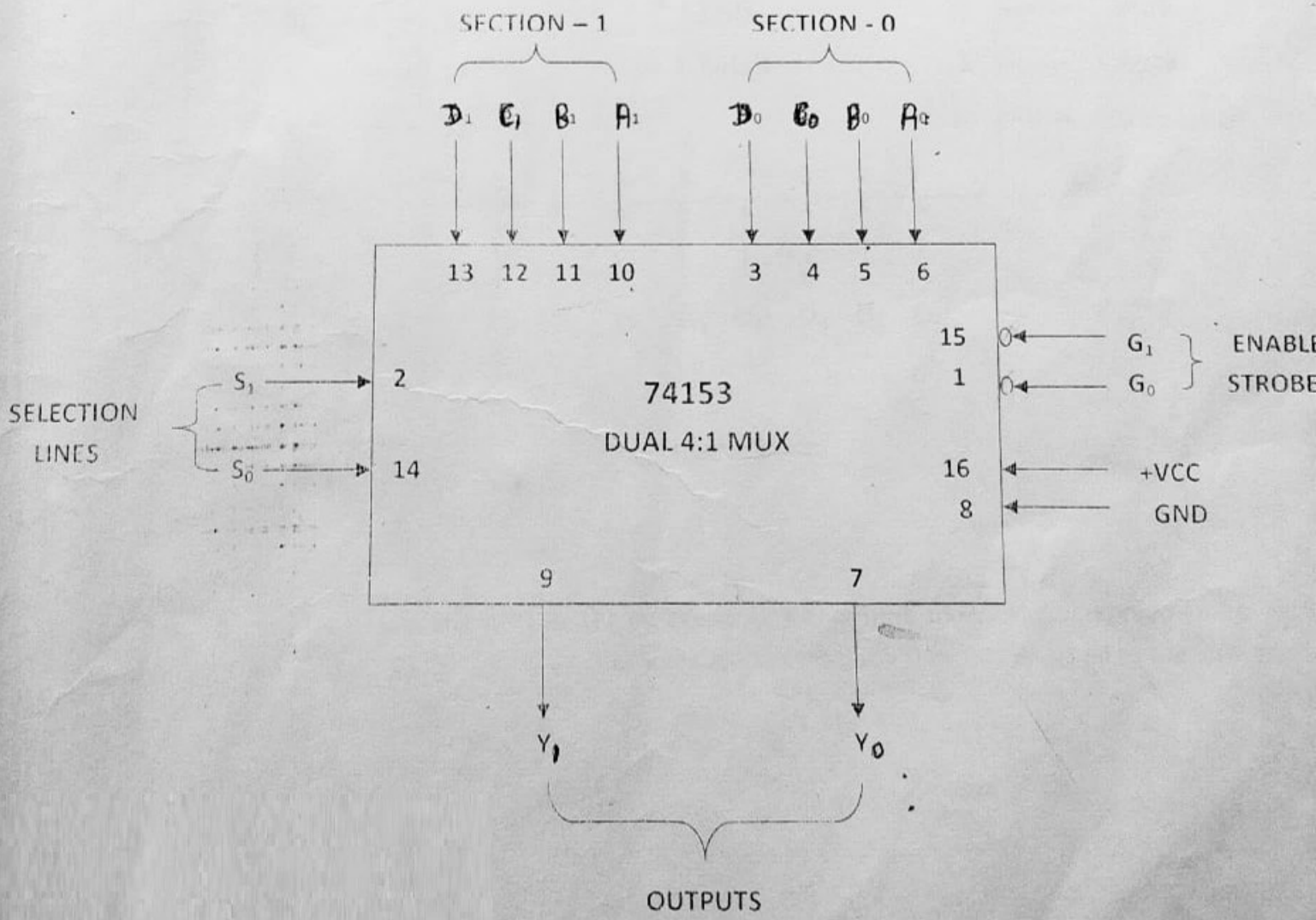


Fig. : BLOCK DIAGRAM OF A MULTIPLEXER (4:1 MUX)

TRUTH TABLE :

SELECTION LINES		INPUT SELECTED				OUTPUT	
S_1	S_0	I_3	I_2	I_1	I_0	Y	
0	0	X	X	X	0	0	I_0
					1	1	
0	1	X	X	0	X	0	I_1
				1		1	
1	0	X	0	X	X	0	I_2
			1			1	
1	1	0	X	X	X	0	I_3
		1				1	

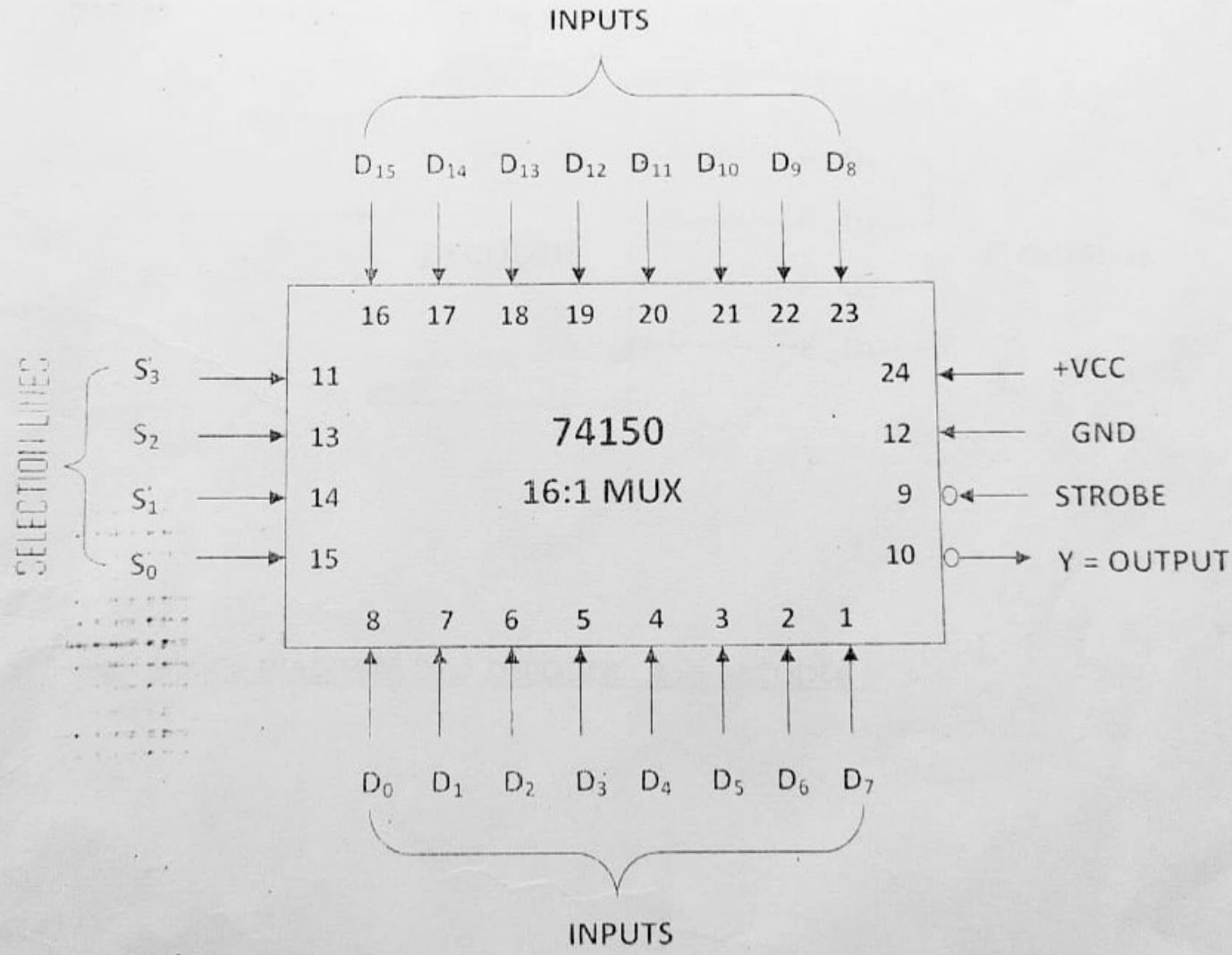
PIN CONFIGURATION OF IC 74153 :



NOTE :

G_0 and G_1 are strobes for selection of Section – 0 and Section – 1 respectively. These are active low enables inputs, so $G_0 = 0$ for Section – 0 and $G_1 = 0$ for Section – 1. A_0, B_0, C_0, D_0 are the inputs and Y_0 is the output for Section – 0. A_1, B_1, C_1, D1 are the inputs and Y_1 is the output for the Section – 1 respectively. S_1 and S_0 are the Selection lines which are common for the both sections.

PIN CONFIGURATION OF IC 74150 :



NOTE :

D_0 – D_{15} are the inputs and Y is the output. Y is active low output, so to get un-complemented output invert the Y output. S3, S2, S1, S0 are the Selection lines. Logic – 0 should be given to the Strobe

EXPERIMENT NO. : 01. (b)

NAME OF THE EXPERIMENT : Familiarity with IC-Chips, b) Decoder.
Truth Table verification and clarification from Data-Book.

COMPONENTS REQUIRED : IC – 74138
IC – 74155

THEORY :

A Decoder is a logic circuit that converts an n-bit binary input code (data) into 2^n output lines such that each output line will be activated for only one of the possible combinations of inputs. In a Decoder, the number of output is greater than the number of inputs.

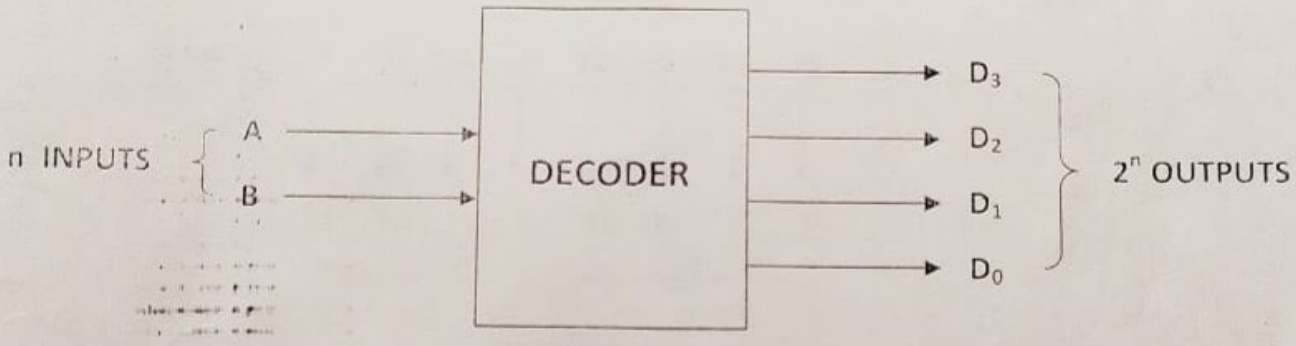
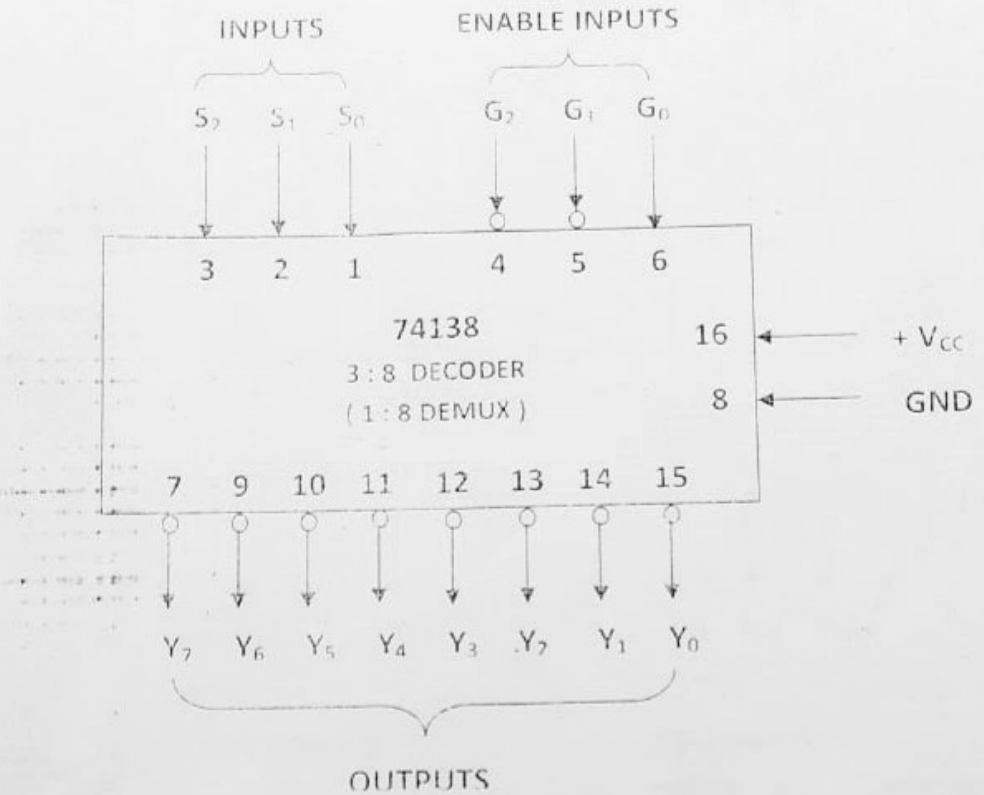


Fig. : BLOCK DIAGRAM OF A DECODER (2 : 4 DECODER)

TRUTH TABLE :

INPUTS		OUTPUTS			
A	B	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

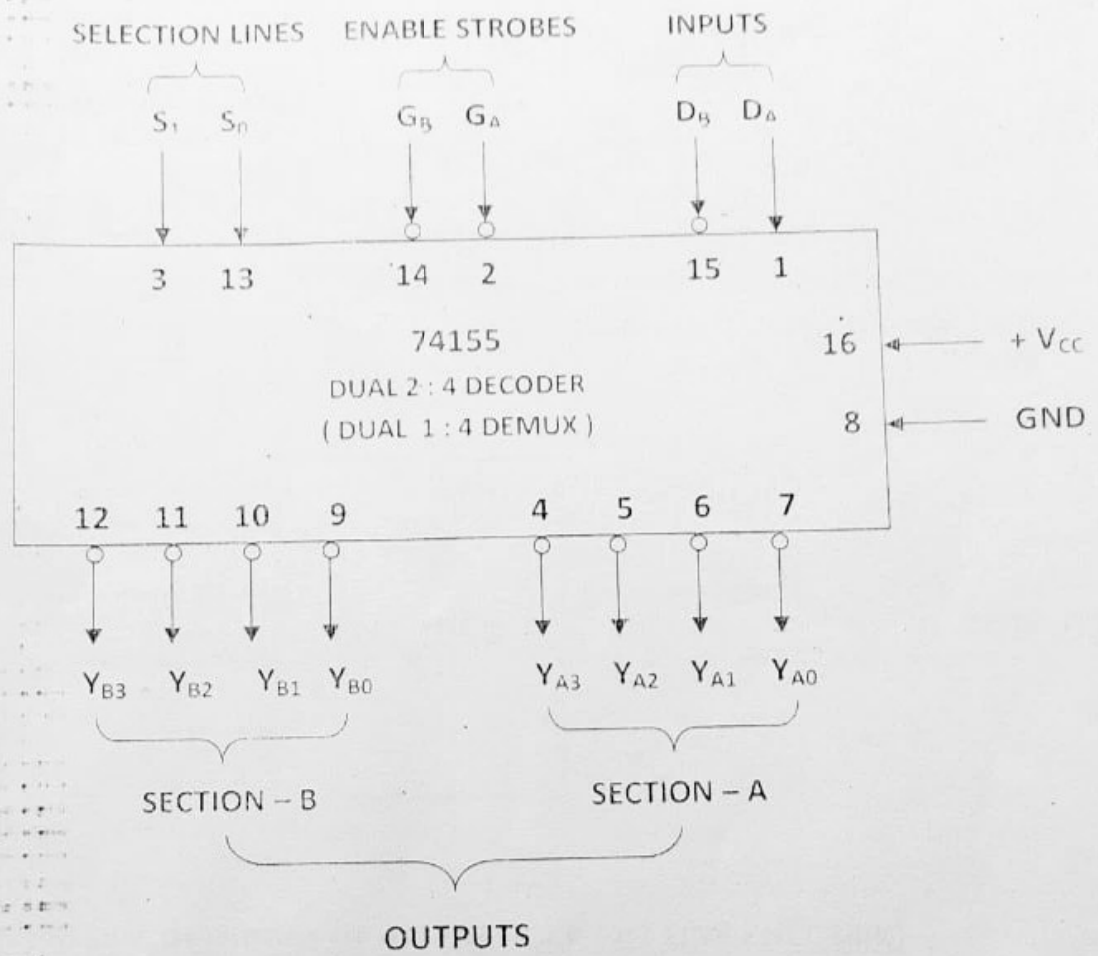
PIN CONFIGURATION OF IC – 74138 :



TRUTH TABLE OF IC – 74138 :

INPUTS			OUTPUTS							
S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

PIN CONFIGURATION OF IC – 74155 :



TRUTH TABLE OF IC - 74155 :

INPUTS		OUTPUTS			
S1	S0	Y_{A3}	Y_{A2}	Y_{A1}	Y_{A0}
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

EXPERIMENT NO. : 01. (c)

NAME OF THE EXPERIMENT : Familiarity with IC-Chips, c) Encoder.
Truth Table verification and clarification from Data-Book.

COMPONENTS REQUIRED : IC – 74147

THEORY :

An Encoder is a digital circuit that performs the inverse operation of a decoder. An Encoder is a combinational logic circuit that converts an active input signal into a coded output signal. In an Encoder, the number of inputs is greater than the number of outputs. It converts 2^n inputs lines into n coded output lines.

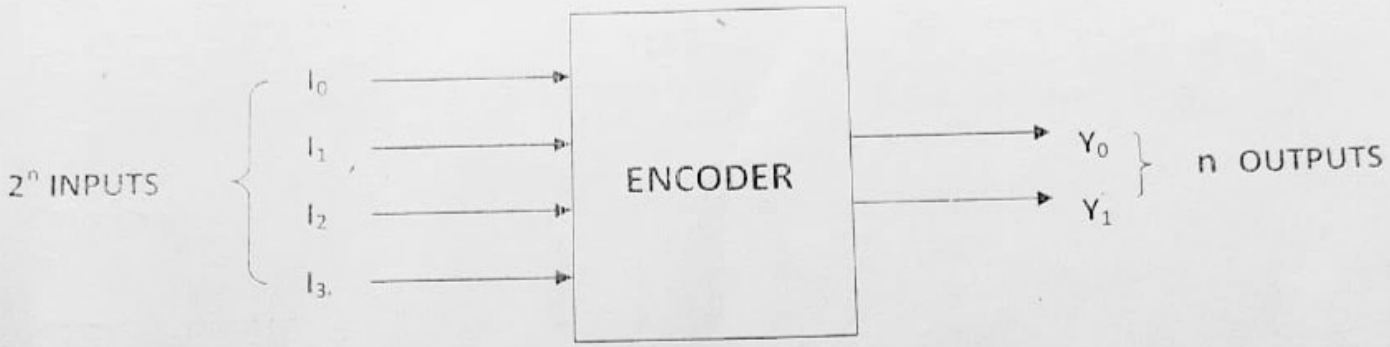
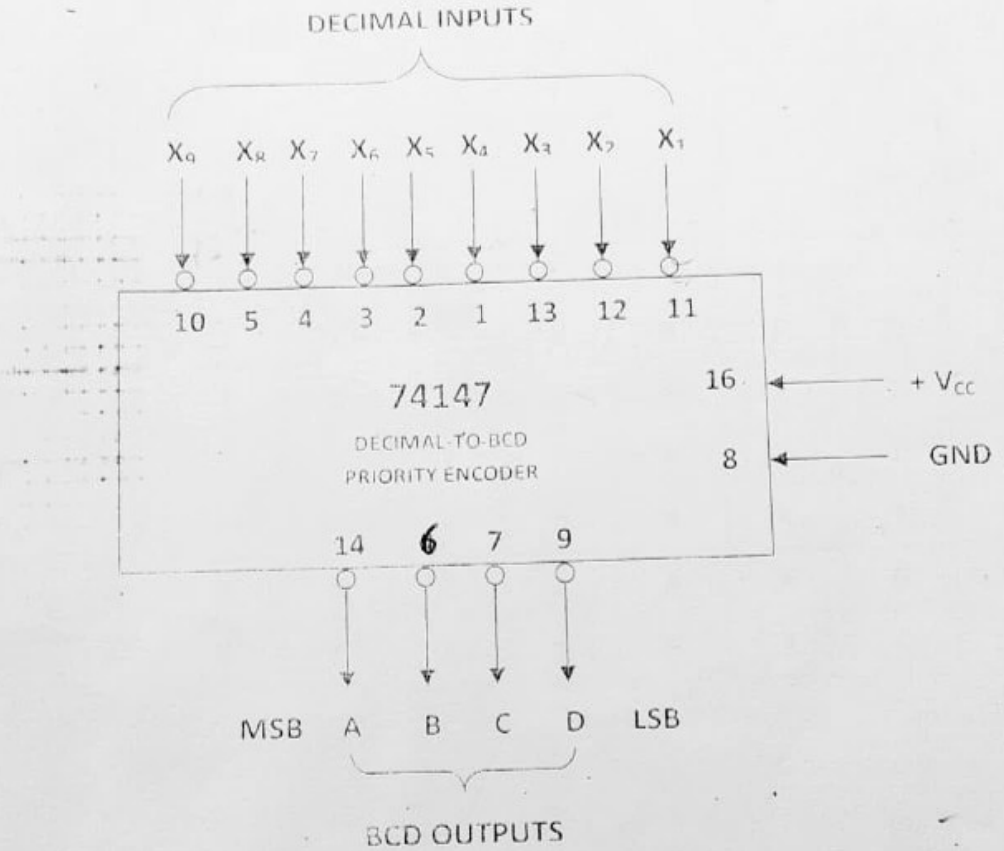


Fig. : BLOCK DIAGRAM OF AN ENCODER (4:2 LINE ENCODER)

TRUTH TABLE :

INPUTS				OUTPUTS	
I_3	I_2	I_1	I_0	Y_1	Y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

PIN CONFIGURATION OF IC – 74147 :



It has 9 active LOW inputs representing the decimal digits, 1 through 9 and produces the inverted BCD code corresponding to the highest order activated input.

When all the inputs (X_1 - X_9) are HIGH, all the outputs are HIGH (i.e. 1111) which is the inverse of 0000, the BCD code for 0. When X_1 is LOW, the ABCD output is 1110, which is the inverse of 0001, the BCD code for 1; when X_2 is LOW, the ABCD output is 1101, the inverse of 0010, the BCD code for 2 and like so on. Hence, the outputs of IC – 74147 will normally be HIGH when none of the inputs is activated. This corresponds to the decimal 0 input condition. Since there is no X_0 input, the encoder assumes the decimal 0 input state when all the inputs are HIGH.

The IC – 74147 is also called a priority encoder because it gives priority to the highest order input. For example, at a particular instant, if both the inputs X_3 and X_5 are activated, then the highest priority of these two inputs (i.e. X_5) is encoded as 1010 which is the inverse of 0101.

TRUTH TABLE OF IC – 74147 :

DECIMAL INPUTS (ACTIVE LOW)									BCD OUTPUTS (ACTIVE LOW)			
X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	A	B	C	D
1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	0	X	1	1	0	1
1	1	1	1	1	1	0	X	X	1	1	0	0
1	1	1	1	1	0	X	X	X	1	0	1	1
1	1	1	1	0	X	X	X	X	1	0	1	0
1	1	1	0	X	X	X	X	X	1	0	0	1
1	1	0	X	X	X	X	X	X	1	0	0	0
1	0	X	X	X	X	X	X	X	0	1	1	1
0	X	X	X	X	X	X	X	X	0	1	1	0

EXPERIMENT NO. : 01. (d)

NAME OF THE EXPERIMENT : Familiarity with IC-Chips, d) Comparator.
Truth Table verification and clarification from Data-Book.

COMPONENTS REQUIRED :
IC – 7485 .

THEORY :

A Magnitude Comparator is a combinational circuit that compares the magnitude of two numbers (A and B) and generates one of the following outputs : A = B, A < B, A > B.

To implement the magnitude comparator, the EX-NOR gates and AND gates are used. The property of the EX-NOR gate can be used to find whether the two binary digits are equal or not, and the AND gates are used to find whether a binary digit is less than or greater than another bit.

IC 7485 is a 4-bit magnitude comparator with two 4 - bit inputs A_3, A_2, A_1, A_0 and B_3, B_2, B_1, B_0 and three outputs, viz. A = B, A <B AND A > B. In addition, it has three cascading inputs which allow several comparators to be cascaded. By cascading several such comparators, any number of bits can be compared.

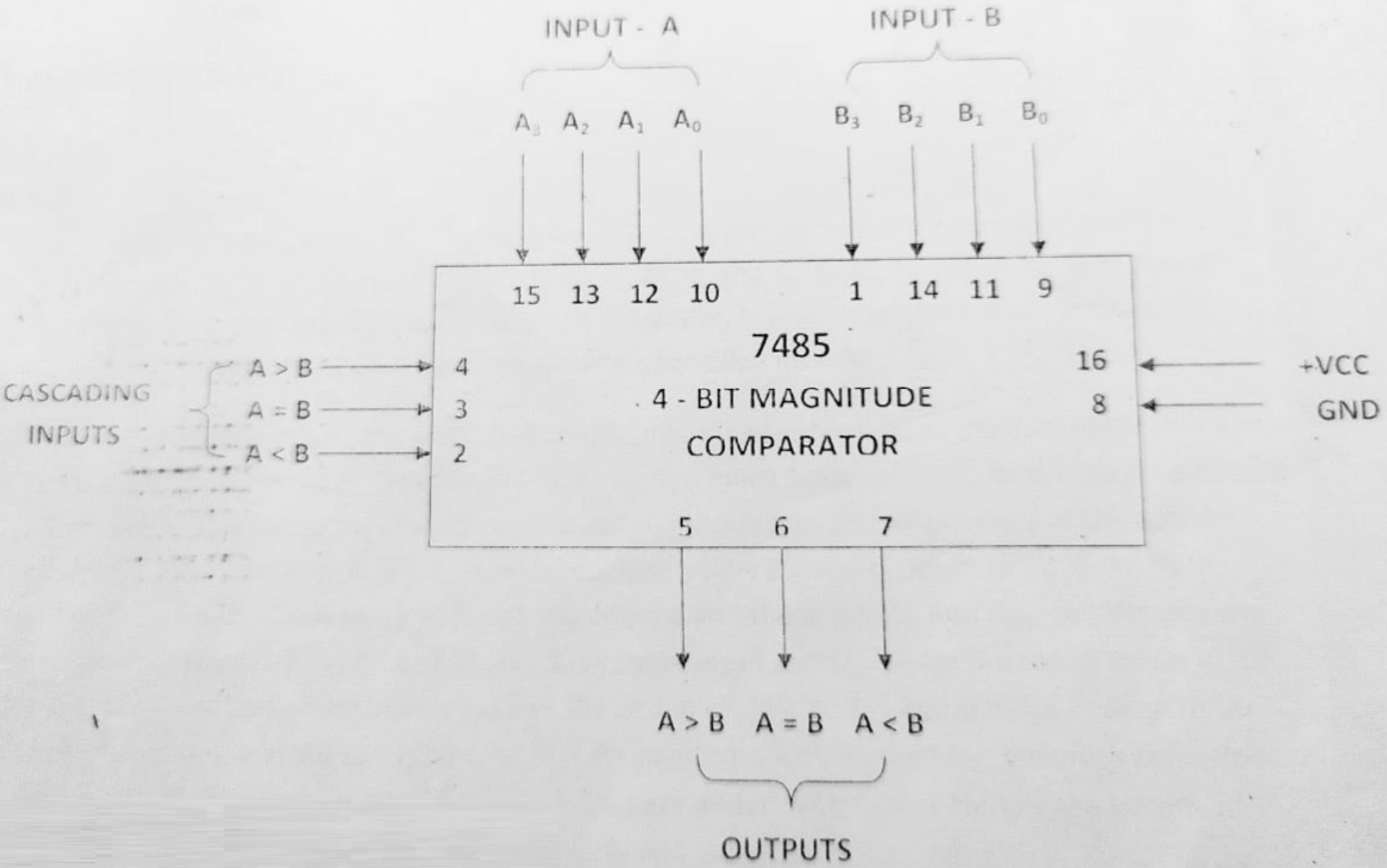
CASCADING OF IC 7485 :

The cascading of two comparators to compare two 8-bit numbers (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0 and B_7, B_6, B_5, B_4, B_3, B_2, B_1, B_0) can be done by connecting A < B, A = B and A > B outputs of the lower order comparator with the respective cascading inputs of the higher order comparator. The cascading input (=) of the lower order comparator must be connected to HIGH, while the cascading inputs (< and >) must be connected to LOW. The A < B, A = B and A > B outputs of the higher order comparator become the cascaded comparator outputs.

APPLICATIONS OF COMPARATORS :

1. Comparators are often used as part of the address decoding circuitry in computers to select a specific input/output device for the storage of data.
2. They are used to actuate circuitry to drive the physical variable toward the reference value.
3. They are used in control applications.

PIN CONFIGURATION OF IC – 7485 :



OUTPUTS

OBSERVATION TABLE :

S.No.	INPUT – A				INPUT – B				OUTPUTS		
	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	A>B	A=B	A<B
1.	0	0	0	0	0	0	0	0	0	1	0
2.	0	0	0	0	0	0	0	1	0	0	1
3.	0	0	0	1	0	0	0	0	1	0	0
4.	0	0	0	1	0	0	0	1	0	1	0
5.	0	0	1	1	0	0	1	0	1	0	0
6.	0	0	1	1	0	0	1	1	0	1	0
7.	1	1	0	0	1	1	1	1	0	0	1

EXPERIMENT NO. : 02

NAME OF THE EXPERIMENT : Design an Adder/Subtractor composite unit.

COMPONENTS REQUIRED : IC – 7483
IC – 7486

THEORY :

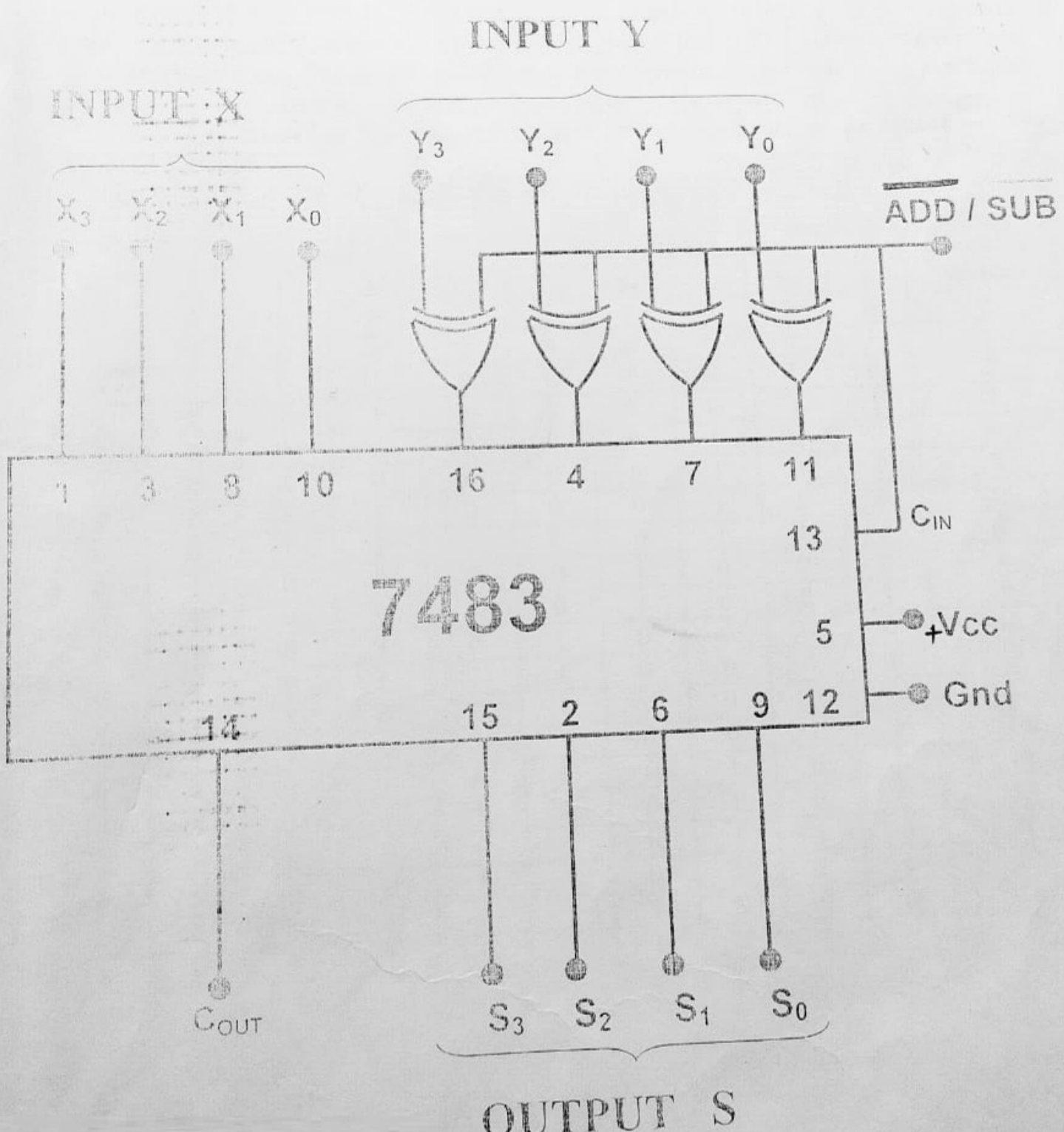
The 4-bit parallel binary adder/ subtractor circuit performs the operations of both addition and subtraction. It has two 4-bit inputs X_3, X_2, X_1, X_0 and Y_3, Y_2, Y_1, Y_0. The $\overline{ADD}$/ SUB control line, connected with C_{in} of the least significant bit of the full-adder, is used to perform the operations of addition and subtraction. The Ex-OR gates are used as controlled inverters.

To perform subtraction, the $\overline{ADD}$/ SUB control input is kept high. Now, the controlled inverter produces the 1's complement of the addend (Y_3, Y_2, Y_1, Y_0). Since 1 is given to C_{in} of the least significant bit of the adder, it is added to the complemented addend producing 2's complement of the addend before addition. Now, the data X_3, X_2, X_1, X_0 will be added to the 2's complement of Y_3, Y_2, Y_1, Y_0 to produce the Sum, i.e., the difference between the addend and the augends, and C_{out}, i.e., the borrow output of 4-bit subtractor. Also, it has S_3, S_2, S_1, S_0 as sum output and C_{out} as carry output. When $\overline{ADD}$/ SUB input is LOW, the controlled inverter allows the added (Y_3, Y_2, Y_1, Y_0) without any change to the input of the full-adder, and the carry input C_{in} of least significant bit of full-adder, becomes zero. Now, the augends (X_3, X_2, X_1, X_0) and addend (Y_3, Y_2, Y_1, Y_0) are added with C_{in} = 0. Hence, the circuit functions as a 4-bit adder resulting in sum S_3, S_2, S_1, S_0 and carry C_{out}.

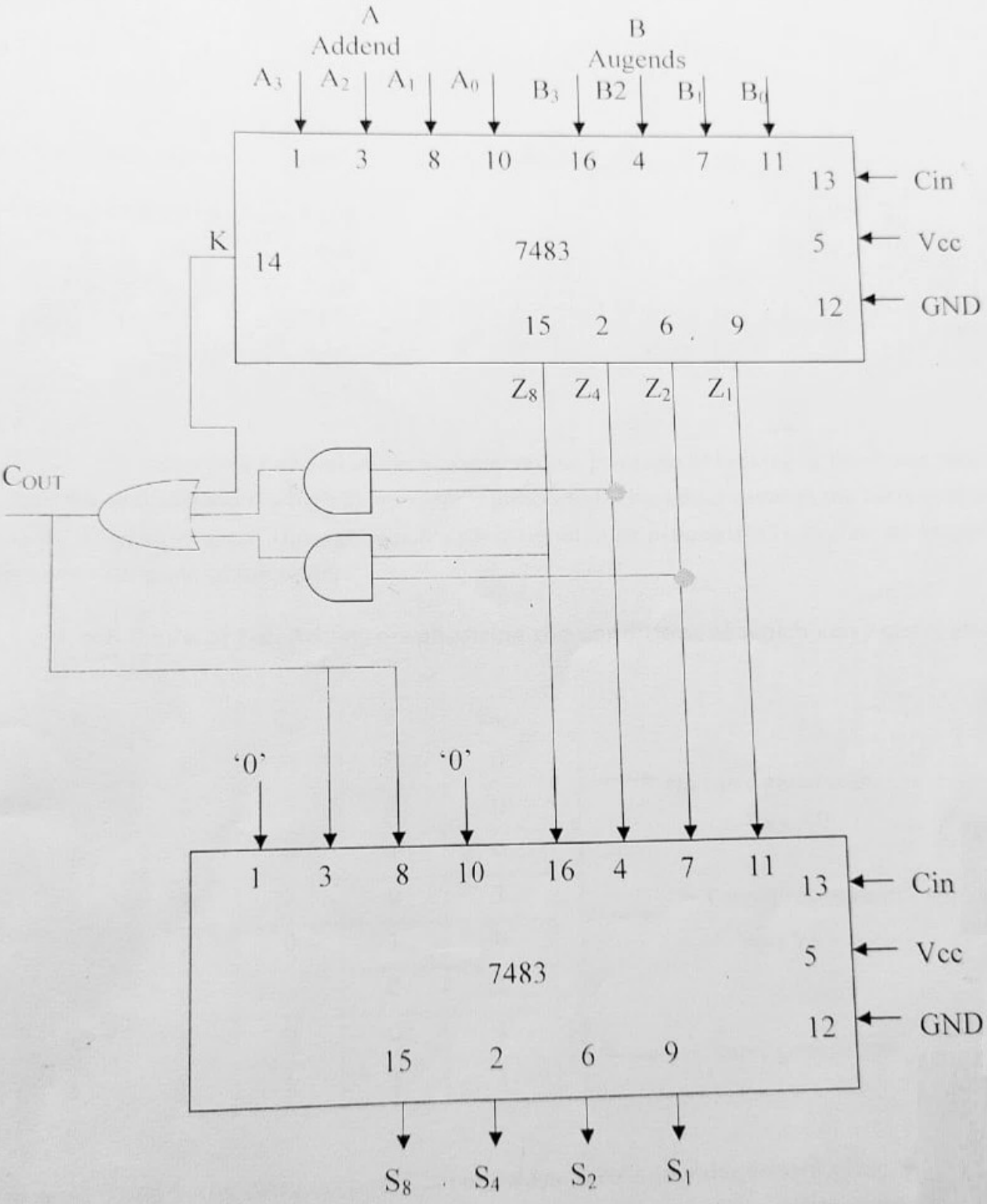
OBSERVATION TABLE :

S.No.	$\overline{ADD}$/ SUB	INPUT – X				INPUT – Y				OUTPUT				
		X_3	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0	C_{OUT}	S_3	S_2	S_1	S_0
1.	0	0	0	0	0	0	0	0	1	0	0	0	0	1
2.	0	0	0	0	1	1	0	0	1	0	1	0	1	0
3.	0	1	0	0	0	1	0	0	0	1	0	0	0	0
4.	0	1	0	1	0	1	1	0	0	1	0	1	1	0
5.	1	0	0	0	0	0	0	0	0	1	0	0	0	0
6.	1	1	0	0	0	0	0	0	1	1	0	1	1	1
7.	1	0	0	0	1	0	0	1	1	0	1	1	1	0
8.	1	0	1	0	1	1	0	1	0	0	1	0	1	1

PIN CONFIGURATION OF ADDER / SUBTRACTOR COMPOSITE UNIT :



CIRCUIT DIAGRAM OF BCD ADDER:



A and B are BCD inputs. Cin is equal to logic-0.

EXPERIMENT NO. – 03

NAME OF THE EXPERIMENT: Design a BCD adder.

IC USED: IC 7483 – 4-bit binary adder.
IC 7408 – Quad 2 i/p AND gate.
IC 7432 – Quad 2 i/p OR gate.

THEORY: In examining the content of the table, it is apparent that when the binary sum is equal to or less than 1001, the corresponding BCD number is identical and therefore no conversion is needed. When the binary sum is greater than 1001, we obtain a nonvalid BCD representation. The addition of binary 6 (0110) to the binary sum converts it to the correct BCD representation and also produces an o/p carry as required.

The condition for a correction and an o/p carry can be expressed by the Boolean function –

$$C = K + Z_8 Z_4 + Z_8 Z_2$$

Binary Sum					BCD Sum					Decimal Number
K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1	
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13
0	1	1	1	0	1	0	1	0	0	14
0	1	1	1	1	1	0	1	0	1	15
1	0	0	0	0	1	0	1	1	0	16
1	0	0	0	1	1	0	1	1	1	17
1	0	0	1	0	1	1	0	0	0	18
1	0	0	1	1	1	1	0	0	1	19

EXPERIMENT NO. : 05

NAME OF THE EXPERIMENT : Use a multiplexer unit to design a composite ALU.

COMPONENTS REQUIRED : IC – 74153
IC – 7404
IC – 7408
IC – 7432
IC – 7486

THEORY :

FUNCTION TABLE :

S. No.	OPERATION SELECT					FUNCTION (F)	OPERATION
	S_3	S_2	S_1	S_0	C_{in}		
1	0	0	0	0	0	F = A + B	ADD
2	0	0	0	0	1	F = A + B +1	ADD WITH CARRY
3	0	0	0	1	0	F = A + $\bar{B}$ = A - B - 1	SUB WITH BORROW
4	0	0	0	1	1	F = A + $\bar{B}$ + 1 = A - B	SUBTRACT
5	0	0	1	0	0	F = A	TRANSFER
6	0	0	1	0	1	F = A + 1	INCREMENT A
7	0	0	1	1	0	F = A - 1	DECREMENT A
8	0	0	1	1	1	F = A	TRANSFER
9	0	1	0	0	X	F = A ^ B	AND OPERATION
10	0	1	0	1	X	F = A $\vee$ B	OR OPERATION
11	0	1	1	0	X	F = A $\oplus$ B	EX - OR OPERATION
12	0	1	1	1	X	F = $\bar{A}$	COMPLEMENT OF A
13	1	0	X	X	X	F = SHIFT A	SHIFT RIGHT A IN F
14	1	1	X	X	X	F = SHIFT A	SHIFT LEFT A IN F

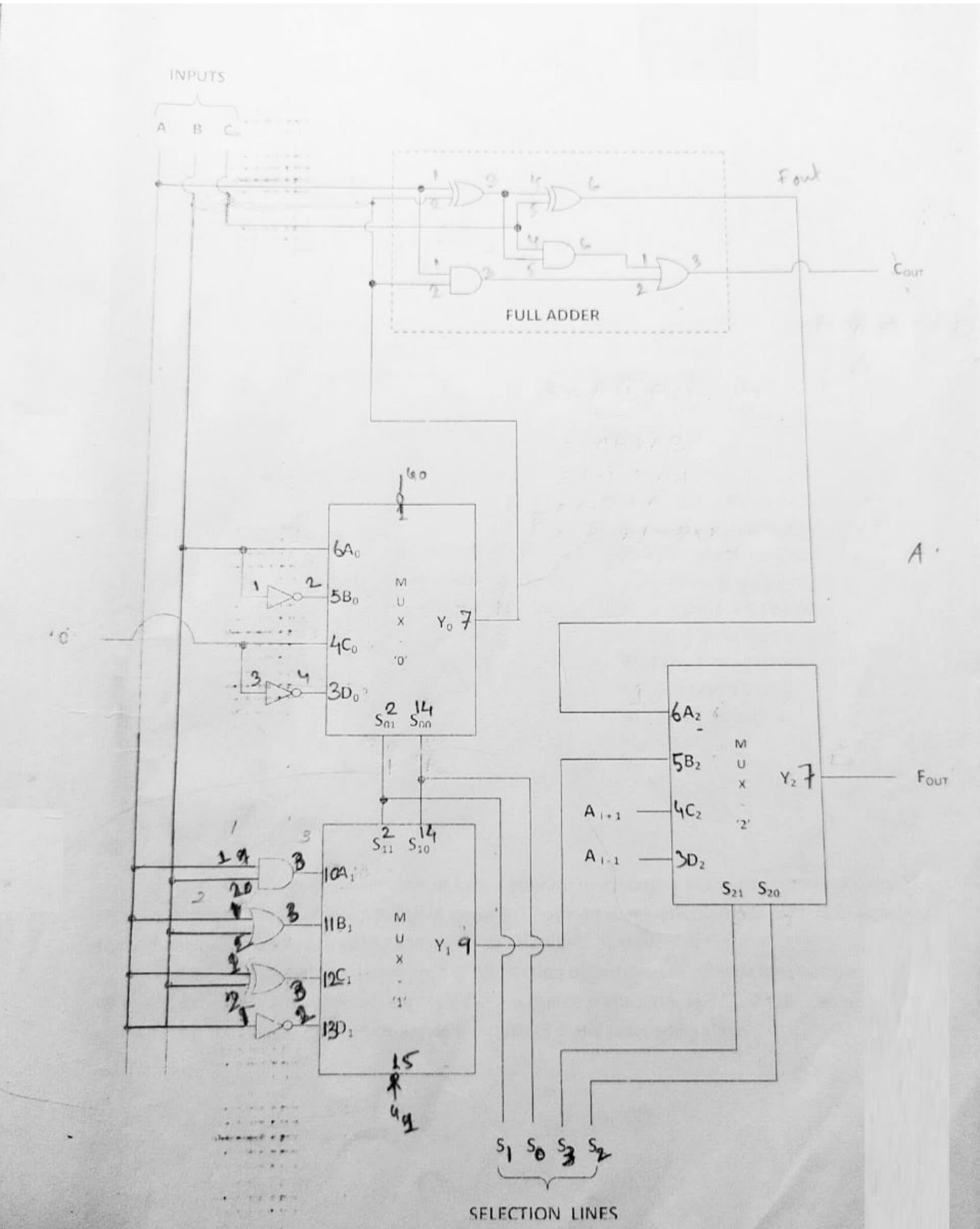


Fig. : Composite ALU unit using MULTIPLEXER

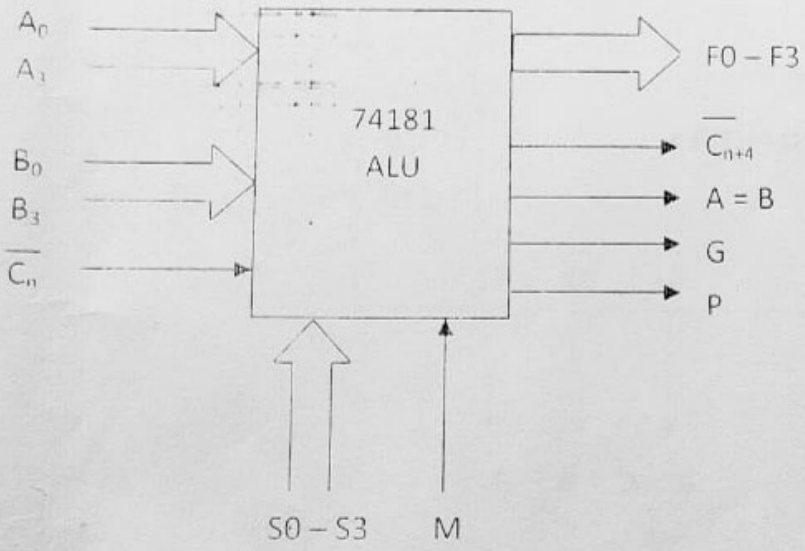
EXPERIMENT NO. : 06

NAME OF THE EXPERIMENT : Use ALU chip for multibit arithmetic operation.

COMPONENTS REQUIRED : IC – 74181

THEORY :

The Arithmetic Logic Unit (ALU) is a widely used combinational circuit, which is capable of performing arithmetic as well as logical operations. This is the heart of any microprocessor and microcontroller. IC 74181 is an example of ALU. It is a 4-bit arithmetic logic unit.



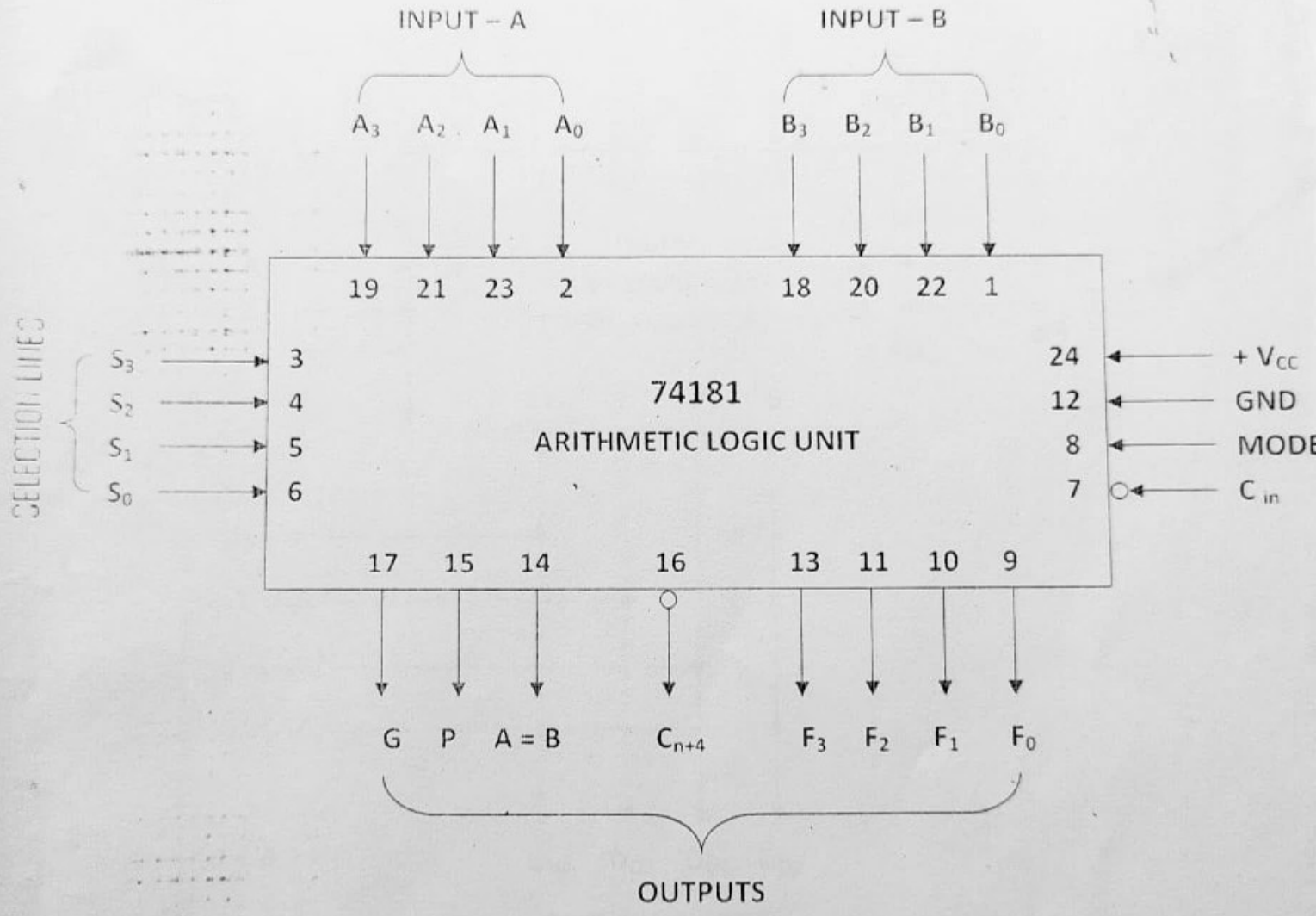
$A_0 - A_3$ & $B_0 - B_3$ = 4-bit binary inputs
$\overline{C_n}$ = Active low carry input
F0 – F3 = 4-bit binary data output
$\overline{C_{n+4}}$ = Active low carry output
A = B = Output for equality
G = Carry generated output
P = Carry propagated output
$S_0 - S_3$ = Select inputs
M = Mode control

Fig. . Functional diagram of IC - 74181

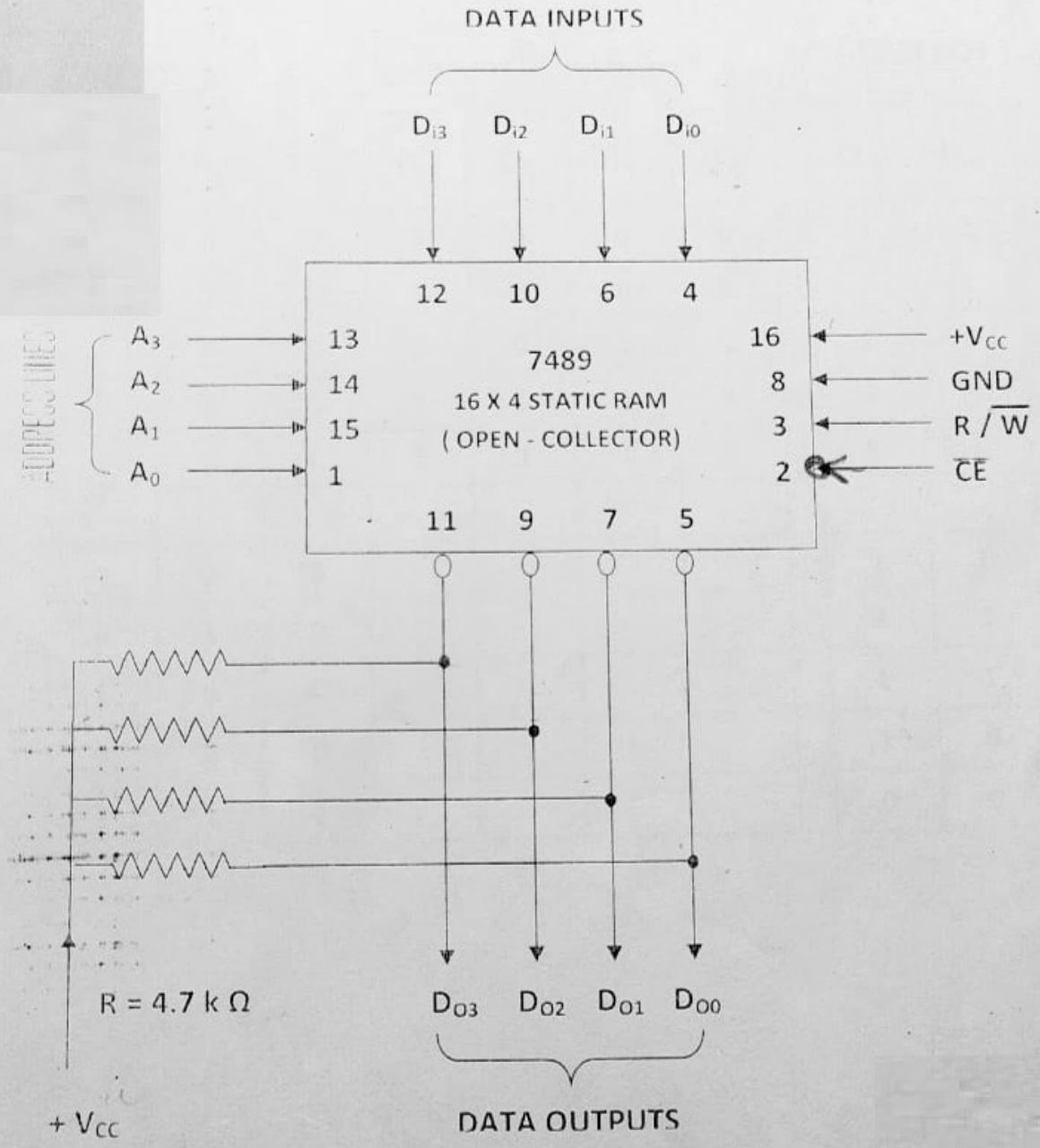
The ALU performs the arithmetic or logical operations according to the mode control signal M. For arithmetic operations, mode control M signal is 0. For logical operations, mode control M signal is 1. S0 – S3 inputs are used to select any one logical or arithmetic operation.

$\overline{C_{n+4}}$ indicates the sign of the output in subtraction operation. Logic 0 indicates positive result and logic 1 indicates negative result expressed in 2 's complement form. The IC - 74181 can be cascaded by connecting the carry output of a stage to the carry-in of the succeeding stage.

PIN CONFIGURATION OF IC – 74181 :



PIN CONFIGURATION OF IC – 7489 :



OBSERVATION TABLE :

$R/\overline{W}$	ADDRESS BUS				INPUT DATA BUS				OUTPUT DATA BUS			
	A_3	A_2	A_1	A_0	D_{i3}	D_{i2}	D_{i1}	D_{i0}	D_{o3}	D_{o2}	D_{o1}	D_{o0}
0	0	0	0	0	0	0	0	0	1	1	1	1
0	0	0	1	0	0	0	0	1	1	1	1	0
0	0	1	0	0	0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	1	1	1	0	0	0
0	1	1	1	1	1	1	1	1	0	0	0	0
1	0	0	0	0					1	1	1	1
1	0	0	1	0					1	1	1	0
1	0	1	0	0					1	1	0	0
1	1	0	0	0					1	0	0	0
1	1	1	1	1					0	0	0	0

EXPERIMENT NO. : 8(a)

NAME OF THE EXPERIMENT : Cascade two RAM ICs for vertical expansion.

COMPONENTS REQUIRED : IC - 7489
IC - 7404
RESISTOR – 4.7 k Ω

THEORY :

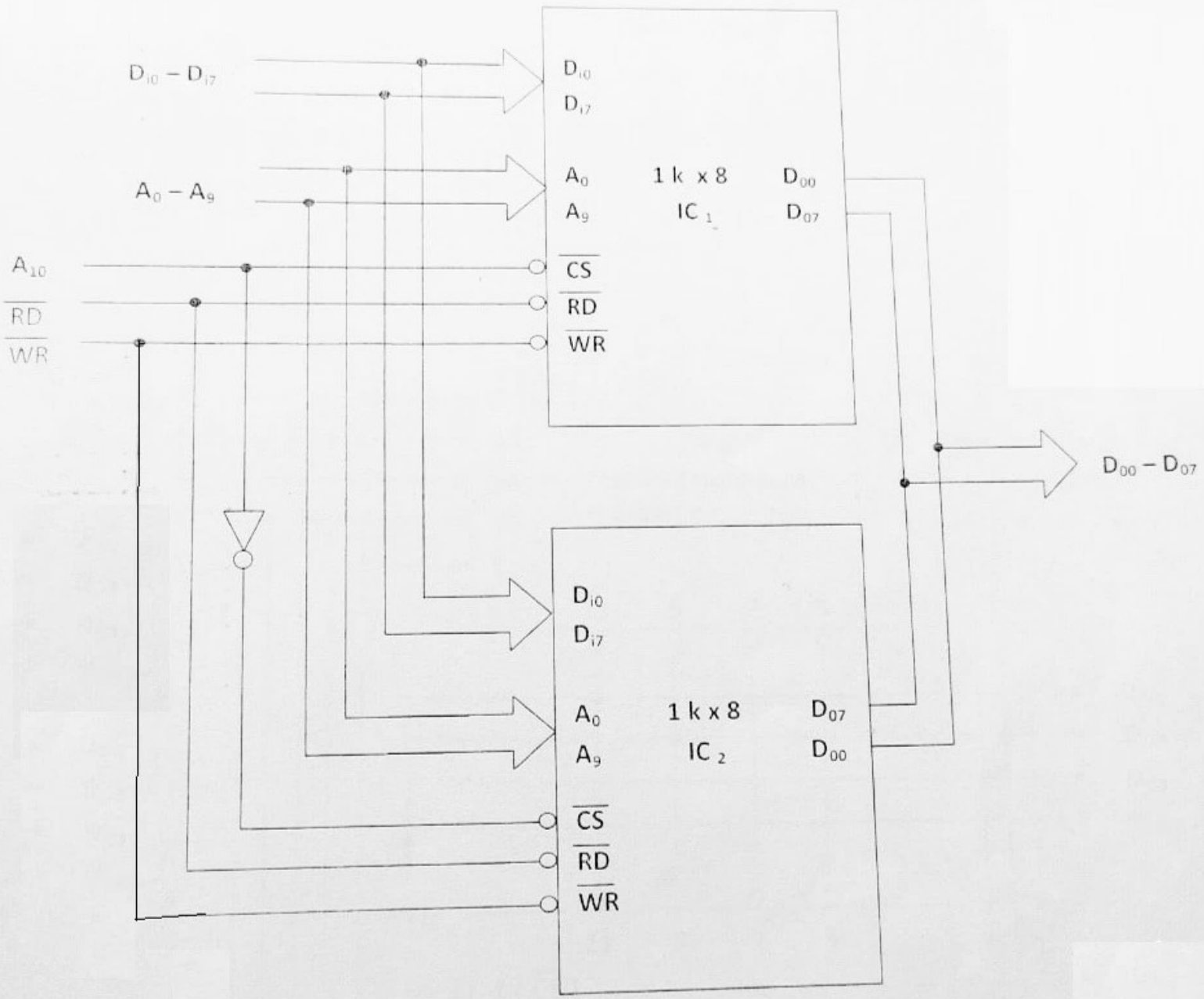
The word capacity of memory is nothing but the number of locations (set of registers). Connecting two or more ICs in series can increase the word capacity of the memory.

Suppose the requirement of word capacity is M_R and the word capacity of available memory IC is M_S, which is less than the requirement. The required number of ICs to get the desired size is M_R/M_S. The connections of the address lines, control signals, and the data lines to get the expanded word capacity are :

a) The corresponding address lines of each ICs are connected together.
b) The $\overline{RD}$ and $\overline{WR}$ signals are also connected together.
c) The corresponding data lines of all ICs are connected together.
d) The chip select signals are generated using a decoder, and separate chip select signals are used to select individual chips.

OBSERVATION TABLE :

$R/\overline{W}$	ADDRESS BUS					INPUT DATA BUS				OUTPUT DATA BUS			
	A_4	A_3	A_2	A_1	A_0	D_{i3}	D_{i2}	D_{i1}	D_{i0}	D_{o3}	D_{o2}	D_{o1}	D_{o0}
0	0	0	0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	1	0	0	0	1	1	1	1	0
0	0	0	0	1	0	0	0	1	1	1	1	0	0
0	0	0	0	1	1	0	1	1	1	1	0	0	0
0	0	0	1	0	0	1	1	1	1	0	0	0	0
1	0	0	0	0	0					1	1	1	1
1	0	0	0	0	1					1	1	1	0
1	0	0	0	1	0					1	1	0	0
1	0	0	0	1	1					1	0	0	0
1	0	0	1	0	0					0	0	0	0



2 k x 8 memory using two 1 k x 8 ICs

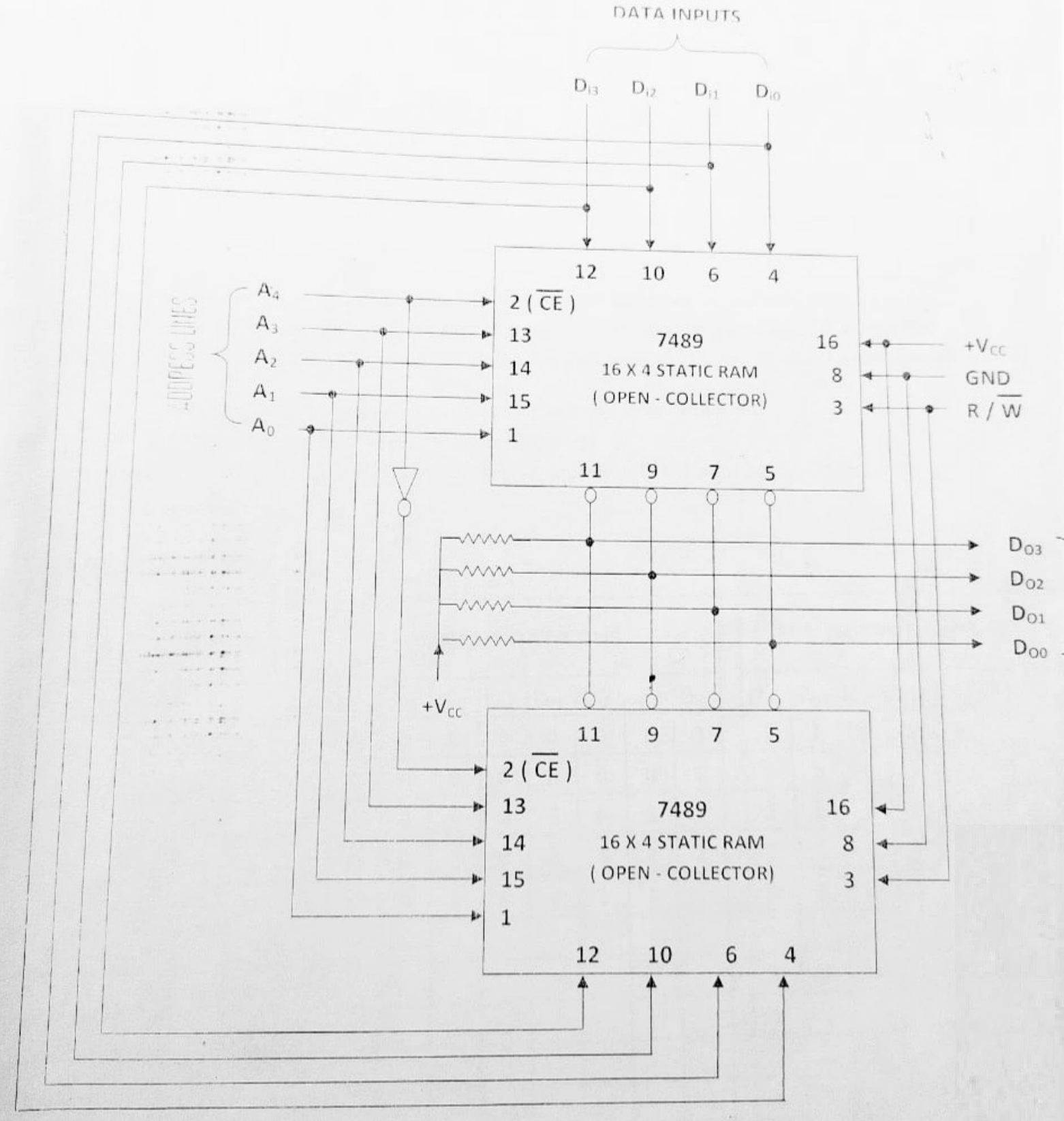


Fig. : 32 x 4 memory using two 16 x 4 RAM ICs

SILIGURI INSTITUE OF TECHNOLOGY

ELECTRONICS AND COMMUNICATION DEPARTMENT

LABORATORY MANUAL

DIGITAL COMMUNICATION

Prepared by: Prof Sudip Ghosh

25/08/15

Prepared on: 25/08/15

Revision No: 00 **Date of revision:** N/A **Revised by:**

SILIGURI INSTITUTE OF TECHNOLOGY

DIGITAL COMMUNICATION LAB (CODE:EC691)

LABORATORY MANUAL

Experiment No. – 1

Experiment Title: Design, implementation and studies of the properties of 15 bitP.N. Sequence using shift register.

OBJECTIVE: This experiment will enable one to understand the pseudo noise(pn)sequence with certain autocorrelation properties.

THEORY :

In spread spectrum system, the signal spreading code is the so called the pseudo noise(PN) sequence which is generally periodic and consists of a periodic coded sequence of 1's and 0's with certain autocorrelation properties. These signals are pseudo random is as much as they appear to be unpredictable to be an outsider, though they appear or can be generated by deterministic means by the person for whom they are intended. When a shift resister has a non-zero initial state and the output is fed back to the input , the unit acts as periodic sequence generation. In general the longest possible sequence from a resister n stages is N= $(2^n - 1)$.The corresponding output is called a maximum length sequence or PN sequence. The names pseudo noise comes from the correlation properties of sequence of N, is very large and T_b is very small, then the pn signal acts essentially like white noise with a small DC component and hence is called Pseudo Noise Sequence.

Property 1: P1

In every period ($p = 2^n - 1$) of PN sequence generated by an n-bit LFSR, the sequence will contain the total number of 1s equal to 2^{n-1}.

Property 2: P2

In every period ($p = 2^n - 1$) of PN sequence generated by an n-bit LFSR, the sequence will contain the total number of 0s equal to $2^{n-1} - 1$.

Property 3: P3

In every period ($p = 2^n - 1$) of PN sequence generated by an n-bit LFSR, the sequence has an occurrence of n number of 1s in succession.

Property 4: P4

In every period ($p = 2^n-1$) of PN sequence generated by an n-bit LFSR, the sequence does not have any occurrence of total number of (n) 0s in succession

Property 5: P5

In every period ($p = 2^n-1$) of PN sequence generated by an n-bit LFSR, the sequence does not have any occurrence of total number of (n–1) 1s in succession

Property 6: P6

In every period ($p = 2^n-1$) of PN sequence generated by an n-bit LFSR, the sequence has an occurrence of total number of (n–1) 0s in succession.

Property 7: P7

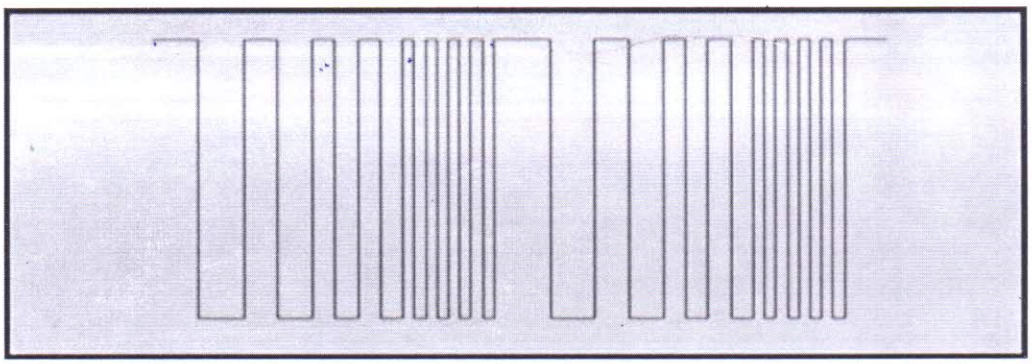
We define the term 'run' in a general way as a succession of items of the same class. In a period of PN sequence the distribution of sequential occurrences of groups of 1s, and 0s (runs property for1kn2≤≤–), is governed by a rule and we present this in the form of the following theorem. THEOREM 1. In every period ($p = 2^n-1$) of PN sequence generated by an n-bit LFSR, the sequence will contain $2k - 1$ runs of $(n - k - 1)$ 1s, as well as 0s, for 1kn2≤≤–.

Property 8: P8

It is also interesting to note that the LFSR generates pulses of different frequencies. The study also, reveals that the pulse width and frequency of different pulses has definite relation with the others as shown in Figure 3. Table 3, describes this property for a PN sequence generated by the LFSR of Figure 2. The generated sequence has periodicity $p = 2^n-1$ with assumption that the clock pulse of LFSR has time period T.

Property 9: P9 (The property of auto-correlation)

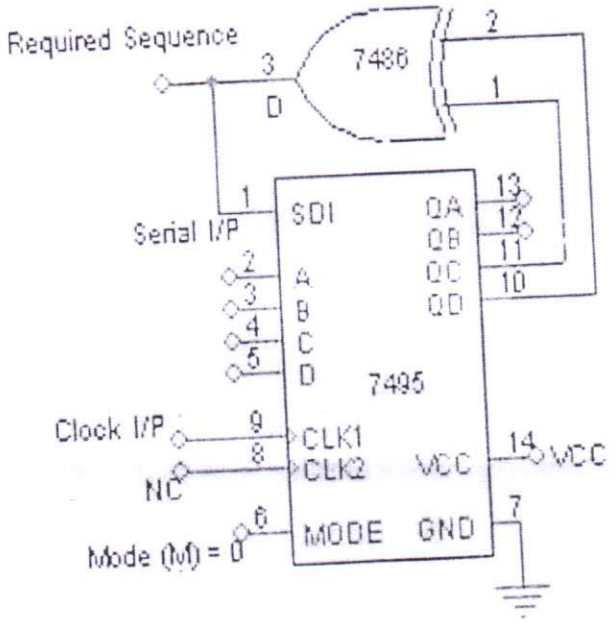
To study the statistical property PN sequences, it is important to analyse them through their correlation functions. Correlation function of two sequences can be described as the comparison of two sequences to see how much they correspond with one another. Various parameters effect the correlation of two sequences including the length of sequence, phase between the sequences, and clock rate of LFSR. The act of correlating a signal through all variations

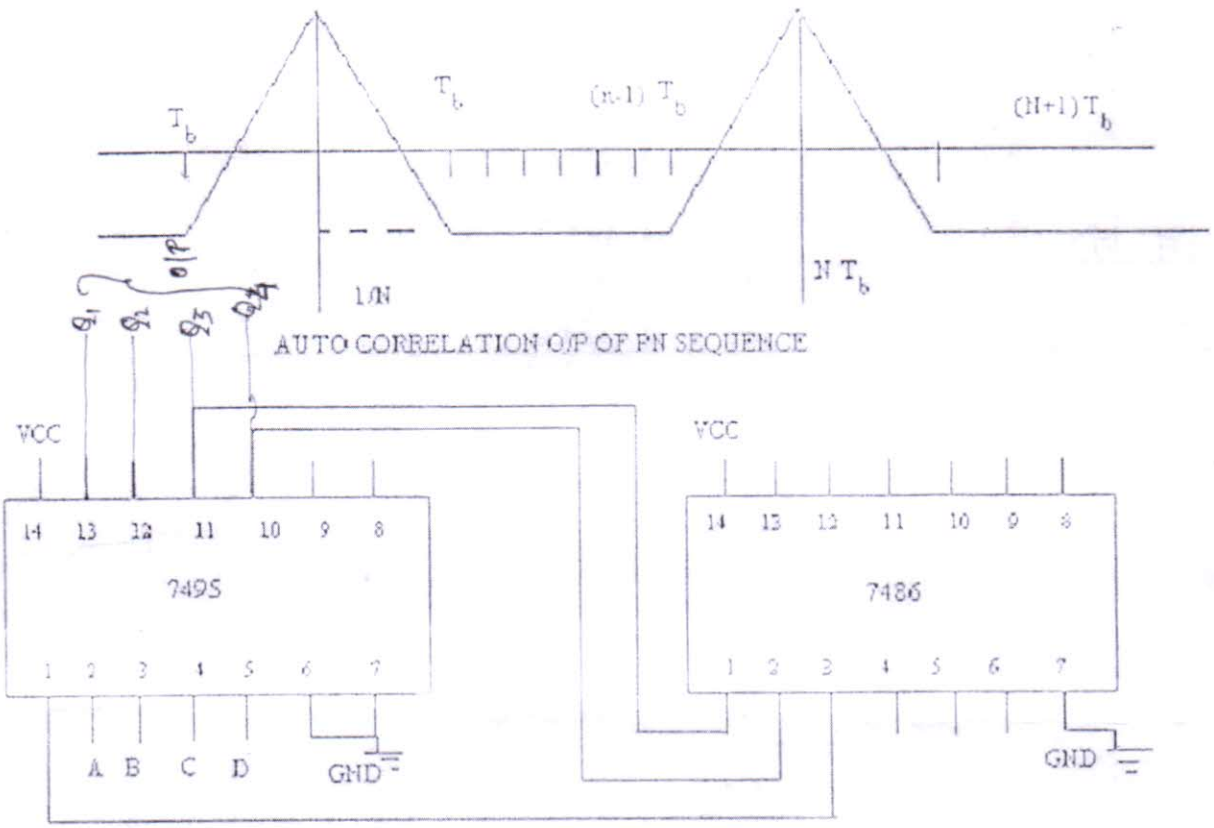


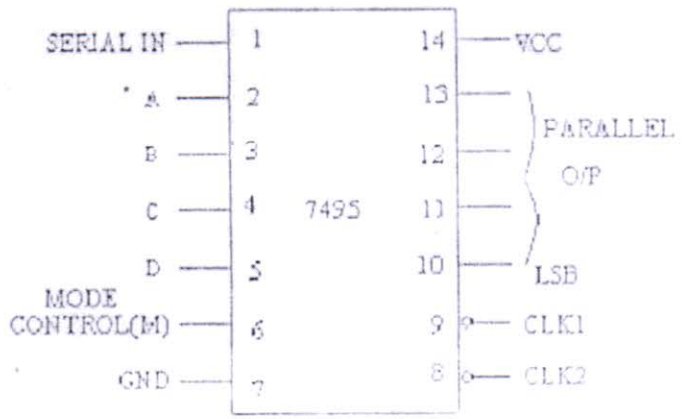
APPARATUS: - IC7495

IC7486

Circuit Diagram




T_b
T_b
$(n-1)\,T_b$
$(N+1)\,T_b$
O/P
1/N
$N\,T_b$
Q_1 Q_2 Q_3 Q_4
AUTO CORRELATION O/P OF PN SEQUENCE
VCC
VCC
14 13 12 11 10 9 8
7495
1 2 3 4 5 6 7
A B C D
GND
14 13 12 11 10 9 8
7486
1 2 3 4 5 6 7
GND


SERIAL IN
A
B
C
D
MODE CONTROL(M)
GND
1
2
3
4
5
6
7
7495
14
13
12
11
10
9
8
VCC
PARALLEL O/P
LSB
CLK1
CLK2

SILIGURI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Digital Communication Lab: Exp no -2

TITLE: **STUDY OF PULSE AMPLITUDE MODULATION AND DEMODULATION**

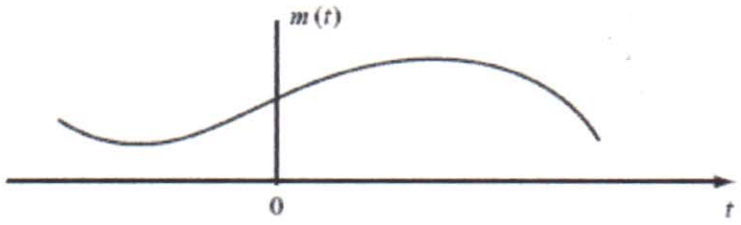
OBJECT: i) STUDY OF DISTORTION FACTOR OF FILTERED RECONSTRUCTED SIGNAL AS A FUNCTION OF SAMPLING FREQUENCY AND AMPLITUDE AND THUS VERIFY THE SAMPLING THEOREM.

EQUIPMENTS REQUIRED:

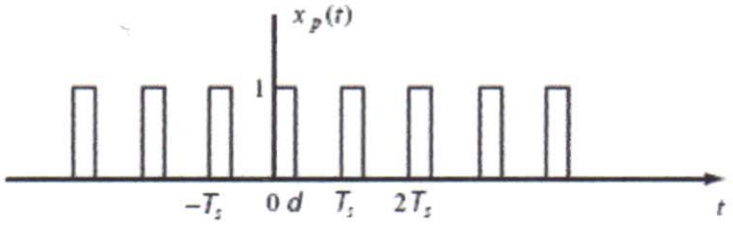
i) Sampling and Reconstruction Trainer Kit- ST-2101
ii) Signal Generator 1 MHz
iii) CRO-20 MHz
iv) Automatic distortion meter-GAD 201G
v) Spectrum Analyzer -3Ghz, GW Instech

THEORY: The Pulse amplitude modulation system is analog system where the trains of Pulse corresponding to the samples of each signal are modulated in amplitude in accordance to the signal itself i.e. the height of the transmitted pulse vary with the amplitude of the message signal. An information signal sent through an ideal (electronic switch) switch which is operated by a control signal, isolated from the information signal, produces a PAM signal. When the switch is open, the voltage is zero; when the switch is closed the out put voltage is equal to the instantaneous signal voltage . The sample width depends upon how long a switch remains closed. The rate at which the signal is sampled is known as the sampling rate or sampling frequency, it is a major parameter which decides the quality of the reconstructed signal. The NYQUISIT CRITERION states that for faithful reconstruction of information signal, sampling frequency should be greater than or equal to twice of the information signal. If the sampling frequency is reduced even further, the sidebands and the information signal will overlap and we cannot recover the information signal by a low pass filtering circuit. This phenomenon is known as fold over distortion or aliasing.

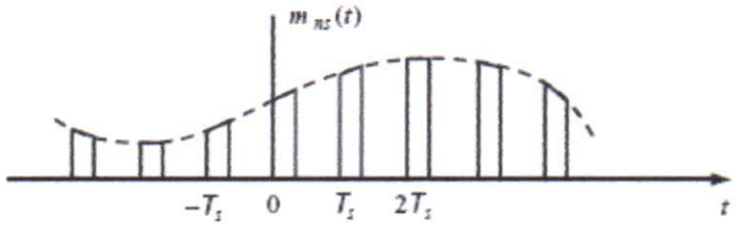
The duty cycle of a signal is defined as the ratio of pulse duration to the pulse repetition period. It is an important parameter in PAM system. The narrower pulses allows to time division multiplex many PAM signal in single channel but it may play a major havoc on the low power signal because of noise, hence a pulse of larger duty cycle is desirous here. In practice an engineering compromise is made between narrower and broader pulse.



(a)



(b)



(c)

BLOCK DIAGRAM:

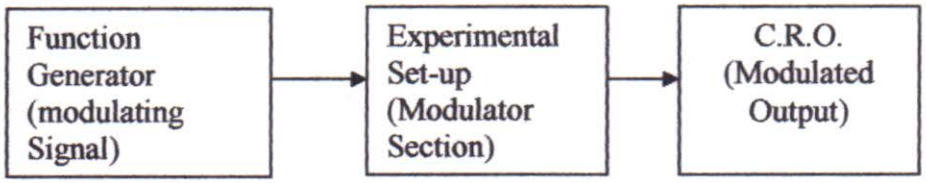
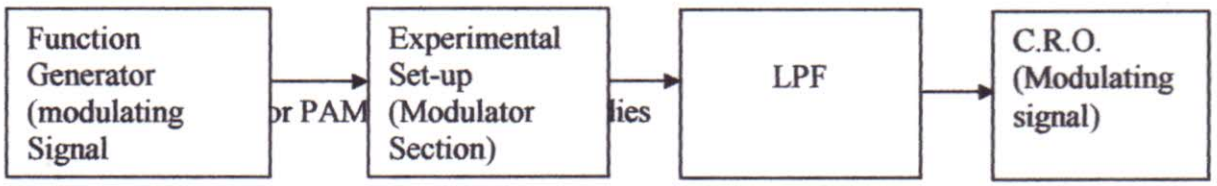


Fig.1.Set up for PAM studies



Experiment procedure :

i)Make the necessary connection in the Trainer Kit ST- 2101 as shown the Fig-

ii) Ensure that EXT/ INT Sampling selector switch is in INT position.

iii) Duty cycle switch to 5 position.

iv) Link 1 Khz sine wave signal to analog input. Select 32Khz sampling rate. Observe analog input at t.p.12 and sampled output at t.p.37 there will be 32 samples for each cycle.

v) Link the Sample output to Fourth Order LPF, now observe Sample output at t.p.37 and the out put of LPF at t.p.46 it is the reconstructed signal of 1Khz sine wave.

v i) Now by successive presses of sampling freq selector switch change the sampling freq to 2,4,8.16 and back to 32 Khz and observe the reconstructed out put and also measure the distortion with distortion meter, note that % of distortion improved as we increase the sampling freq.

vii) Now apply 2Khz 2 volt Peak sine wave signal from a signal generator and set sampling freq to 8 Khz , observe the wave from at t.p46, decrease the sampling rate to 4Khz and then to 2Khz observe the distorted wave from at LPF's output (t.p46) This is due to under sampling of the input i.e overlooking the nyquist criteria and thus the out put is distorted even though the signal lie below the cut-off freq of the filter.

vii) Now set sampling freq at 32 Khz and vary the input analog signal (increase from 2Khz to 10 Khz) and measure the distortion at LPF's output (First at second order filter then at fourth order filter).Again fix input signal freq at 4 Khz and sampling freq 32Khz now vary the amplitude of the signal input and measure the distortion at LPF's output. (First at 2^{nd} Order filter then at 4^{th} Order filter) Tabulate at the data.

viii) Study the spectrum of modulated signal with spectrum analyzer.

Observation Table: Table No 01

Input Signal (Khz)	Sampling freq (Khz)	% of distortion

Table no 02 :

Input Signal (Khz)	Sampling freq (Khz)	% of distortion

Table No 03

Input Signal (Khz)	Input signal amplitude	Sampling freq (Khz)	% of distortion

CONCLUSION:-

Questions:-

1. State the Sampling theorem.
2. What is interpolation.
3. What is Aliasing.
4. What are the different sampling techniques.
5. What do you understand by Aperture effect

SILIGURI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Digital Communication Lab: Exp no. 3

TITLE: TO STUDY PULSE CODE MODULATION (PCM)

OBJECTIVE: 1) To study Analog to digital & Digital to analog conversion.
2)To study and measure quantization error.
3) To measure Bit rate and bandwidth requirement of the System.

EQUIPMENTS REQUIRED:

S.NO	APPARATUS NAME	SPECIFICATION
1.	Experimental kit	ST-2103 & ST-2104
2.	Function generator	1MHZ,SCIENTIFIC
3.	C.R.O.	20MHZ,SCIENTECH
4.	Digital multimeter	

THEORY:

The PCM transmitter samples the analog input, quantizes it and codes it by analog to digital conversion. As it is known, the binary number system consists of binary digits '0' and '1'. The group on n bits is called as **word** and is used to distinguish a code from other. The range of decimal numbers represented by such n bits code is equal to 2^n (including 0) e.g. If we take an 8 bit work, the number or different codes possible is equal to $2^8 = 256$ i.e. we have 0 to 255 code levels available.

This range can be used to indicate any range of voltage. The process of allocating the binary values to each sample taken in PAM system is called as **quantization.** Every binary number indicates one level. Since binary value changes in discrete steps and is not continuous like analog waveform, some distortion creeps in at the time of value assignment. The range of binary values used is design feature of the system and depends upon the amplitude range of the signal and the accuracy of the conversion to be achieved.

Block diagram explanation:

In PCM generator of figure the signal x(t) is first passed through the low-pass filter of cutoff frequency f_m Hz. This low-pass filter blocks all the frequency components which are lying above f_m Hz.

This means that now the signal x(t) is band limited to f_m Hz. The sample and hold circuit them samples this signal at the rate of f_s. Sampling frequency f_s is selected sufficiently above nyquist rate to avoid aliasing i.e.,

$$Fs > 2fm$$

In figure 01 the output of sample and hold circuit is denoted by x(nTs). This signal x(nTs) is discrete in time and continuous in amplitude. A q-level quantizer compares input x(nTs) with its fixed digital levels. It assigns any one of the digital level to x(nTs) with its fixed digital levels. It then assigns any one of the digital level to x(nTs) which results in minimum distortion or error. This error is called **quantization error.** Thus, output of quantizer is a digital level called $x_q(nTs)$.

Now, the quantized signal level $x_q(nTs)$ is given to binary encoder. This encoder converts input signal to 'v' digits binary word. Thus $x_q(nTs)$ is converted to 'v' binary bits. This encoder is also known is digitizer. These 'v' binary digits are converted to serial bit stream to with a parallel to serial converter to generate single baseband signal. The output f PCM generator is thus a single base band signal of binary bits.

An oscillator generates the clocks for sample and hold circuit and parallel to serial converter.

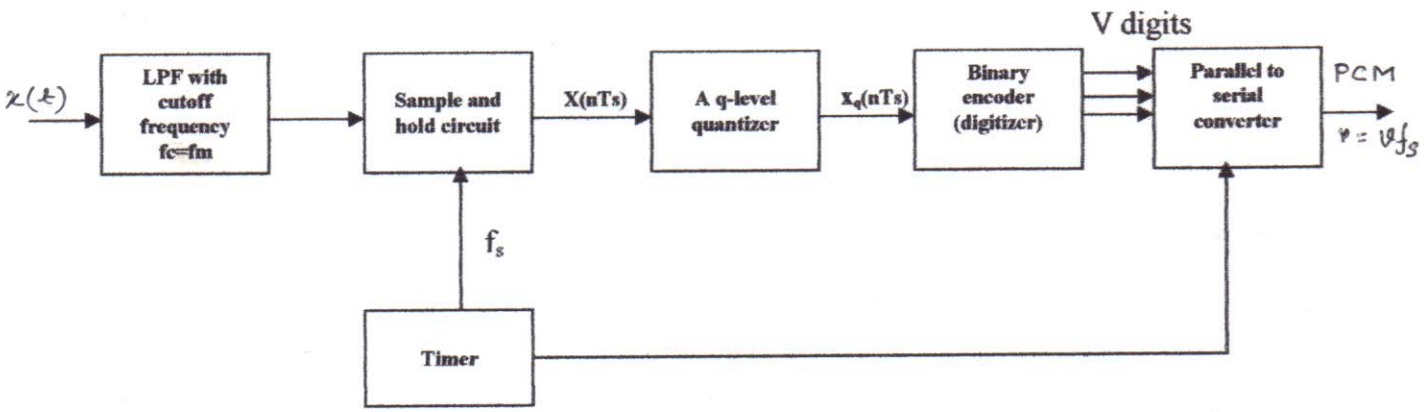


Fig- 1 **PCM transmitter**

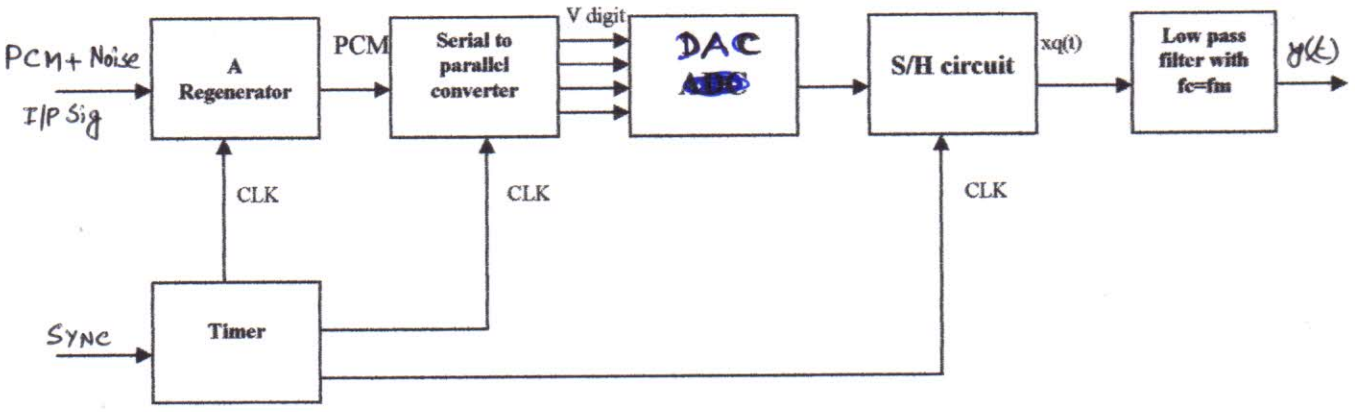
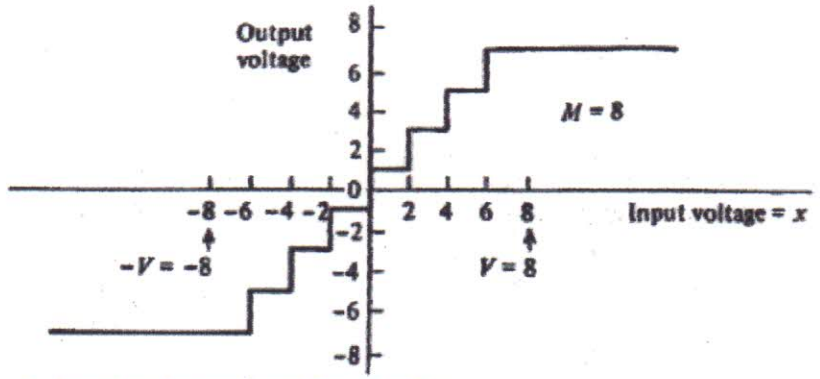
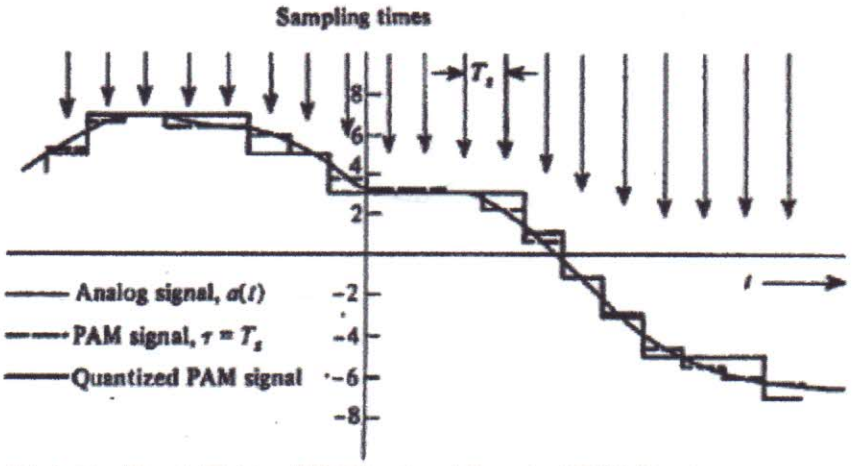


Fig- 2 **PCM receiver**

The regenerator at the start of PCM receiver, reshapes the pulse and remove the noise. This signal is then converted to parallel digital words for each sample. Now, the digital word is converted to its analog value denoted as $x_q(t)$ with the help of a sample and hold circuit. This signal , at the output of S/H circuit is allowed to pass through a Low Pass reconstruction filter to get the appropriate original message signal denoted byy(t).



(a) Quantizer Output-Input Characteristics



(b) Analog Signal, Flat-top PAM Signal, and Quantized PAM Signal

Fig-

TABLE 1:

INPUT SIGNAL (DC INPUT)	OUTPUT OF ADC (D_0 –D_7)	OUTPUT OF LATCH (D_0 –D_7)	DEMODULATED OUTPUT

TABLE 2:

INPUT SIGNAL (AC INPUT) F_M	V_M	**DEMODULATED OUTPUT**	**% OF DISTORTION**

Transmission Bandwidth in a PCM system:

Let us assume that the quantizer use 'v' number of binary digits lto represent each level. Then, the number of leves that may be represented by 'v' digits will be $\mathbf{q= 2^v}$

Here 'q' represents total number of digital levels of a q-level quantizer. For example, if v= 4 bits, the total number of levels will be, $q=2^4= 16$ levels

Each sample is converted to 'v' binary bits. i.e.,
Number of bits per sample = v.
We know that,
Number of samples per second = fs
Therefore, number of bits per second = number of bits per samples X Number of samples per second
= v bits per sample X fs samples per second

These number of bits per second is known as signaling rate or **bit rate of PCM system.** And is denoted by 'r'

Signaling rate or bit rate in PCM r =v fs

Where fs> 2fm
Also, since bandwidth needed for PCM transmission is given by half of the signaling rate therefore, we have
Transmission Bandwidth in PCM,

$BW \geq \frac{1}{2} r$

But $r = v\ fs$

Therefore, $BW > \frac{1}{2} v\ fs$

Again, since $fs \geq 2fm$

Hence, **the require expression for bandwidth of a PCM system is**

$BW \geq v\ fm$

COMMENTS/CONCLUTION:

PROCEDURE TO CARRY OUT THE EXPERIMENT ON TRAINER KIT ST : 2103 & 2104 :-

(1) Ensure the following initial conditions on the ST2103 Trainer.

(A) MODE switch in FAST position.

(B) DC.1 & DC.2 Controls in Function Generator Block, Fully Clockwise.

(C) ~1KHz & ~2KHz signal controls set to 10Vpp.

(D) PSEUDO - RANDOM SYNC CODE GENERATOR switched OFF.

(E) ERROR CHECK CODE SELECTOR switches A & B in A = 0 & B=0 Position (OFF Mode)

(F) ALL SWITCHED FAULTS OFF.

(2) Connect on ST2103 :

DC.1 output to CH.0 input

DC.2 output to CH.1 input

(3) Turn ON the Power. With the help of Digital Voltmeter / Oscilloscope, adjust the DC.1 amplitued control until the DC.1 output measures 0V. The accuracy should be within +/-20mV.

Turn the DC.2 amplitude control, Fully Counter Clockwise.

(4) Observe the output on the A/D Converter Block LED's (D0 TO D6). The LED's represent the state of the binary PCM word allocated to the PAM sample being processed.

An illuminated LED represent a '1' state, while non illuminated LED indicates a '0' state. D6 is the MSB & D0 is the LSB.The LED output looks as follows.

D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0

This output is the digital representation of 0V input to CH.0

(5) Adjust the DC.1 amplitude control clockwise to increase the amplitude & anticlockwise to decrease it.

Try varying the D.C. input from + 5 V to - 5 V in steps of 1V. Take care that the input value is within the specified range of +/- 20mV

Observe that the output for +5V is as follows :

D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1

Where for the negative values it is less than 1000000. For -5V the output is as follows :

D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0

This is obtained at the approximately full anti clock wise position of the DC Control.

(6) Turn the DC1 control fully anti clockwise and repeat the above procedure by varying DC2 control. Check that the digital code for the set voltage value is identical to that of the DC 1 setting.

Once again take a precaution of maintaining the set input within +/- 20mV range of the specified voltage.

(7) Switch 'OFF' the Trainer.

Disconnect the DC 1 & DC 2 supply from CH.0 & CH.1

Connect ~1KHz signal to CH.0 & 2KHz signal to CH.1 input.

(8) Trigger the dual trace oscilloscope externally by the CH.1 signal available at t.p. 12.

Observe the signal at CH.0 & CH1 sample output (t.p.5) with reference to the SC Signal (t.p.7) on the second trace. Give a special attention to the phase relation between the two signal.

(9) Now connect the oscilloscope channel 1 to CH 1 sample (t.p.6) sketch the three waveforms with utmost importance to the relationship between the three waveforms.

(10) Connect Oscilloscope channel 1 input to SC test points (t.p. 7) & Oscilloscope channel 2 input to EC test point (t.p. 8)

Observe the phase relation between the two SC & EC test point. Notice that EC goes HIGH at the end of conversion & remains latched until next SC Pulse.

Mode 1

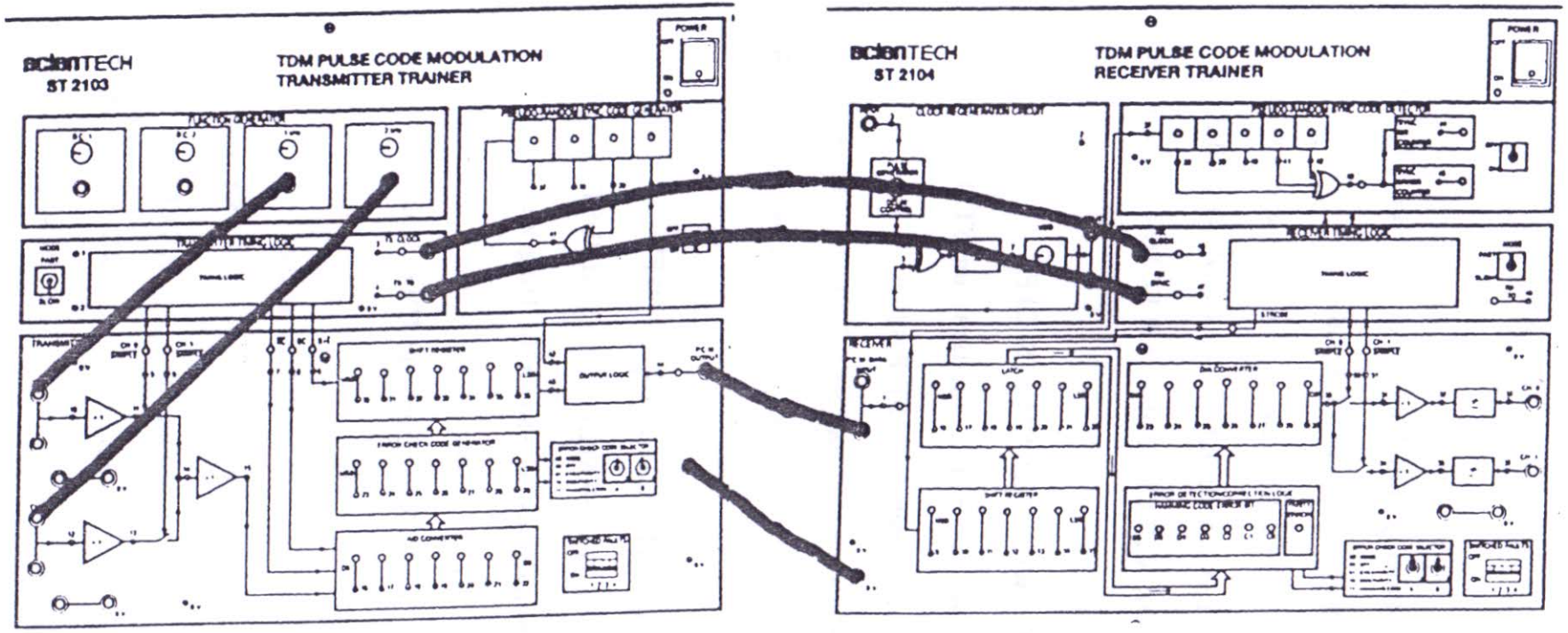


Diagram 3

(1) **Set up following initial conditions on the ST2103 trainer :**

(A) MODE Switch in FAST Position.

(B) DC.1 & DC2 Controls in Function Generator Block fully clockwise.

(C) PSEUDO RANDOM SYNC CODE GENERATOR switched 'OFF'.

(D) ERROR CHECK CODE SELECTOR Switches A & B in A=0 & B=0 Position.

(E) ALL SWITCHED FAULTS OFF.

(2) **Set up following initial conditions on ST2104 trainer :**

(A) MODE Switch in FAST Position.

(B) PSEUDO RANDOM SYNC CODE DETECTOR Switched OFF.

(C) ERROR CHECK CODE SELECTOR switches A & B in A=0 & B=0 Position.

(D) ALL SWITCHED FAULTS 'OFF'.

(E) PULSE GENERATOR DELAY ADJUST Control in Fully Clockwise Position.

(3) **Make connections as shown in Diagram 3 :**

(A) ON ST2103 trainer :

(I) ~KHz Signal to CH.0 Input.

(II) ~2KHz Signal to CH.1 Input.

(B) Between ST2103 & ST204 trainer :

ST2103	ST2104
(1) TX.CLOCK Output	RX.CLOCK Input
(2) TX.TO Output	RX SYNC Input
(3) PCM Output	PCM. DATA Input

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Digital Communication Lab: Exp no. 4

TITLE: STUDY OF MANCHASTER CODING TECHNIQUE

OBJECT: To study Manchaster coding and decoding technique, and study the nature of wave form and spectrum.

EQUIPMENTS REQUIRED:

S.NO	APPARATUS NAME	SPECIFICATION
1.	Experimental kit	ST 2106 & ST2107
2.	Function generator	1MHZ,SCIENTIFIC
3.	C.R.O.	20MHZ,SCIENTECH
4.	Spectrum Analyzer	3 Ghz GW Instech

THEORY:

The main disadvantage with NRZ (L), NRZ (M) or RZ format of coding is there inability to provided reliable clock synchronization information to the receiver clock. Biphase codes overcome this problem by providing the transition in both 0's and '1's.

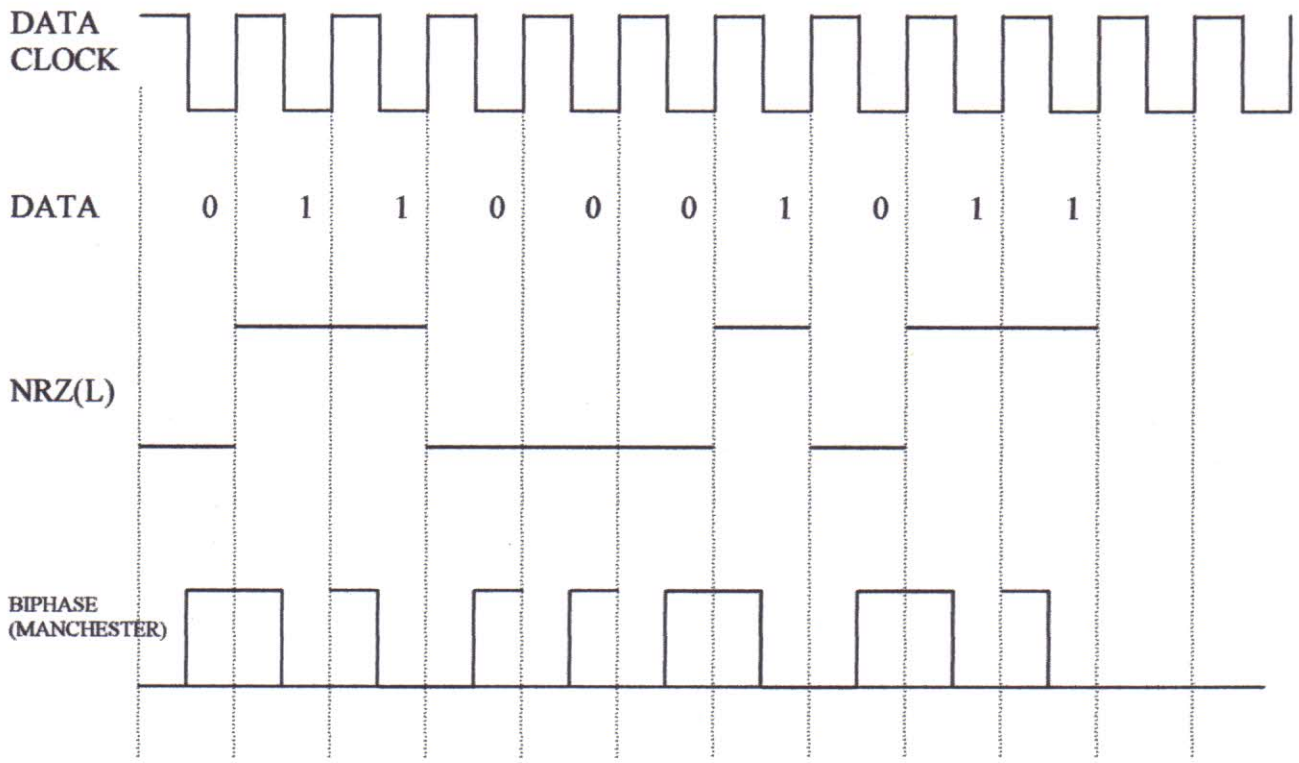
The two most common biphase codes in practice are Biphase (Manchester) and Biphase (Mark) codes. Also these codes are independent of the DC Levels i.e. they have zero d.c. component.

BIPHASE (MANCHESTER) CODING:

THE ENCODING RULES FOR Biphase (Manchester) code are as follows. A data '0' is incoded as a low level during first half of the bit time and a high level during the second half.

A data '1' is encoded as a high level during first half of the bit time and a low level during the second half. Thus string of 1's or 0's as well as any mixture of them will not

pass any synchronization problem in receiver. Fig 1 shows the Biphase (Manchester) waveform for a given data stream.



BANDWIDTH:

The Biphase (Manchester) code always contains at least one transition per bit time, irrespective of the data being transmitted. Hence the maximum frequency of the Biphase (Manchester) code is equal to the data clock rate when a stream of consecutive data '1' and '0' is transmitted. Therefore the required bandwidth is same as that of the RZ code and double as that of the NRZ (L) code.

DC LEVEL :-

Since the Biphase (Manchester) code has a high level for half of each data bit time and low level for second half irrespective of the data. The effective d.c. level of the Biphase coded waveform is zero. This allows it to be used in a.c. coupled communication systems.

PROBLEM IN DECODING:

This form of coding certainly provides plenty of rising edges for clock synchronization but they do not all occur at same time e.g. we have a rising transition at the start of code for data '1' where as for data '0' we have it at the midway of the data bit time. This causes confusion in the clock regeneration circuit.

To overcome this, we employ a special Biphase Clock Recovery Circuit which can be synchronized by the rising edge occurring at either time.

Rest of the decoding is same as for the RZ code. Since the valid data is carried for in first half of each clock period, we ensure that the regenerated receiver clock's rising edge occurs at this time.

Procedure:- See at last page.

Questions:-

1. What is the encoding rules for Bi-phase Manchester Code.
2. Name two most common bi-phase codes.
3. What is the bandwidth requirement in Manchester code.
4. What is the effective d.c level of the Manchester code
5. What is the main advantage of this coding format.

(1) The experiment makes use of four trainers namely **ST2103, ST2104, ST2106 & ST2107.** **ST2103** TDM Pulse Code Modulation Transmitter Trainer serves as a data source while ST2104 TDM Pulse Code Modulation Receiver Trainer serves as analog signal recoverer. ST2106 serves as data formatting (Conditioning) device while ST2107 reformats (decondition) the data.

ST2103 & ST2106 Trainers serves as transmitter for our system & ST2107 & ST2104 Trainer serves as receiver.

(2) Ensure that all trainers are switched OFF, until the complete connection are made.

(3) Check ST2104 Trainer's CLOCK REGENERATION CIRCUIT Set up for correct operation as given in experimentation 1 of ST2103 / 4 work book

(4) Set up the following conditions on ST2103 trainer

(A) **MODE** switch set in **FAST** position.

(B) **PSEUDO - RANDOM SYNC CODE GENERATOR** switched **'ON'.**

(C) **ERROR CHECK CODE SELECTOR** switches **A & B in A=0 & B=0** Positions.

(D) All switched faults 'OFF'

(5) Set ST2106 trainer's MODE switch in position ' 1 '

(6) Set up following conditions on ST2104 trainers :

(A) **MODE** switch set in **FAST** position

(B) **PSEUDO - RANDOM SYNC CODE DETECTOR IN 'ON'** position.

(C) **ERROR CHECK CODE SELECTOR** switch A & B IN A = 0 & B = 0 position.

(D) **All switched faults kept 'OFF'**

(7) Make the following connections between ST2103 A, ST2106 trainers.

ST2103 Trainer **ST2106 Trainer**

(A) TX CLOCK OUTPUT (t.p. 3) TO TX .CLOCK INPUT

(B) PCM OUTPUT (t.p. 44) TO TX .DATA INPUT

(8) Connect the TX TO OUTPUT (t.p 4) on ST2103 trainer to external trigger input of the oscilloscope. Set to negative edge triggered mode in oscilloscope. It may be necessary to adjust the trigger level manually to obtain a stable waveform.

(9) On ST2103 trainer make following connections :

(A) DC 1 to CH 0 INPUT

(B) CH 0 input to CH 1 input

This is done to supply the same voltage level to each of the two time division multiplexed channels. Thus we are able to get the same data stream for any time frame.

(10) Make the rest of the connections as shown in configuration Fig 3.

(11) Switch 'ON' the power

(12) On ST2103 trainer adjust the D.C.1 potentiometer until the 7 bit code displayed on A / D CONVERTER LED's is

D6	D5	D4	D3	D2	D1	DO
0	1	0	0	0	1	1

(13) Observe the DATA CLOCK output at t.p 4 on ST2106 trainer's DATA FORMAT block with oscilloscope. Adjust the oscilloscopes time base & position control until each rising edge of data clock coincides with one of scope's. vertical graticule line as shown in **Figure 4.** Each main division on scope's horizontal axis now represent one data bit time. Adjust the trigger level (manually, if necessary, to obtain a stable trace.) This sets convenient reference against which to observe the other wave forms.

(14) Use the other trace of your oscilloscope to observe the Biphase (Manchester) waveform at t.p. 8. of ST2106. This is identical to the waveform shown in Figure 1.

To view the complete waveform adjust the timebase & X-Position controls until you have exactly two clock pulse within each of the oscilloscope's vertical graticule lines. Monitor Biphase (Manchester) waveform again.

(15) Readjust the timebase & X-Position controls to original set-up again. Switch 'OFF' the power. As it has been stated earlier in the Biphase (Manchester) theory section, we need a BIPHASE CLOCK RECVERY CIRCUIT, on ST2107 trainer. The function of BIPHASE CLOCK RECOVERY CIRCUIT is that it accepts rising edges at both the centre of a bit interval as well as at the start. Its output is a square wave whose period is equal to one bit interval & where as rising edge occupies one quarter (1/4) of the way through the bit interval.

(16) Make the following ADDITIONAL connections. (See Fig 11) Biphase (Manchester) output (t.p. 8) on ST2106 to Biphase CLOCK RECOVERY CIRCUIT input (t.p. 31) on ST2107.

(17) Make the following connections between **ST2107 and ST2104** trainers.

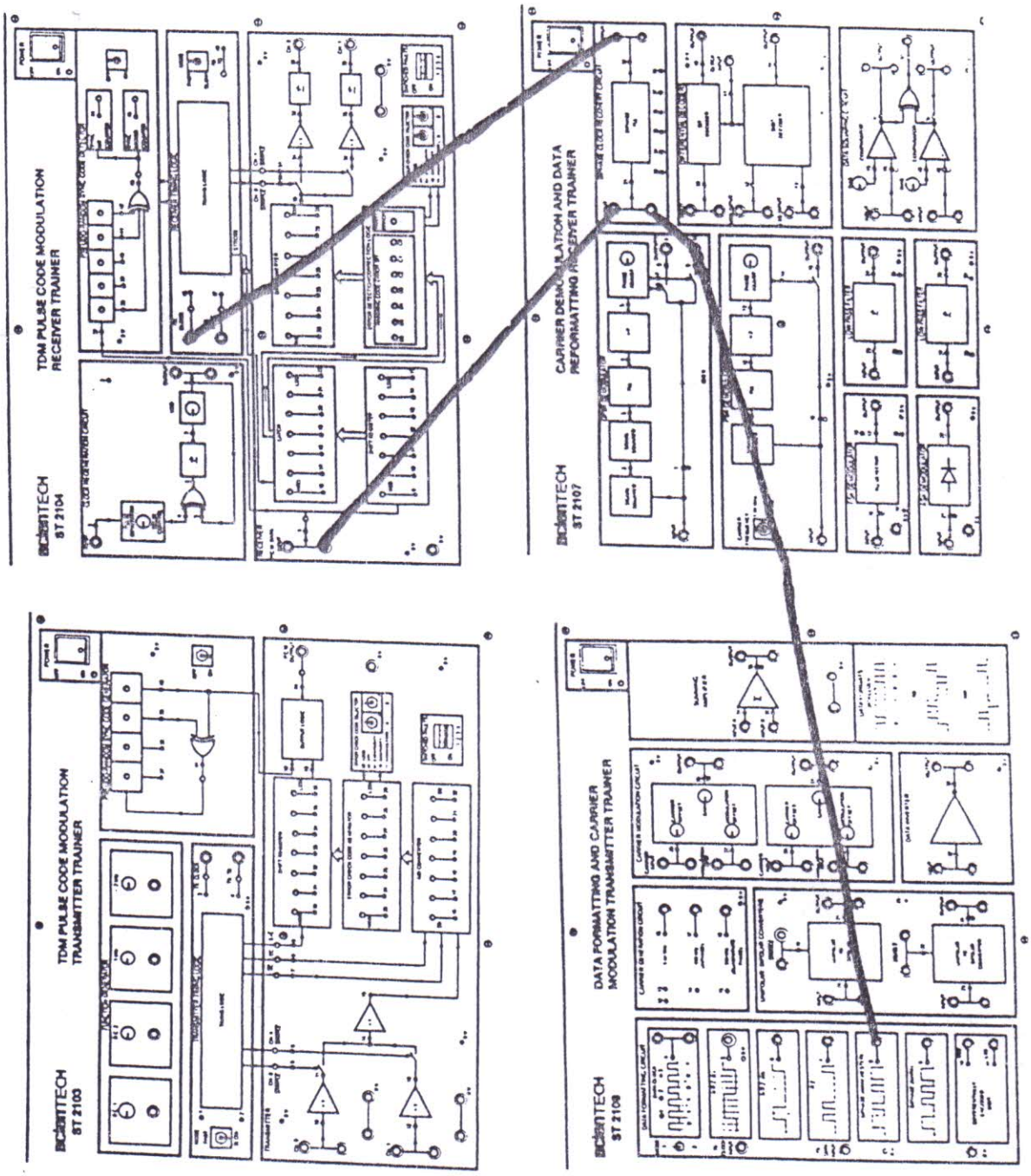
(A) Biphase Clock Recovery Circuit input (t.p. 31) On ST2107 to PCM DATA input (t.p. 1) on ST2104.

(B) Biphase Clock Recovery Circuit output (t.p. 32) on ST2107 to 'RX CLOCK input (t.p. 46) on ST2104. See **Fig 11.**

(18) Switch 'ON' the trainers. On close observation of the regenerated data output. We see that the frequency of the signal is same but is quarter cycle delayed as compared to the data clock.

(19) Switch OFF the trainers. Disconnect the CH.0 & CH.1 inputs & connect 1KHz output to CH.0 & 2KHz output to CH.1

(20) Turn ON the power. Observe the two channel outputs on ST2104 trainer (t.p. 33 & 36). Also observe they are independent is found, it can be removed by adjusting the PULSE GENERATOR DELAY ADJUST potentiometer control slightly.



THEORY OF DATA FORMATTING

The symbols '0' and '1' in digital systems can be represented in various formats with different levels & waveforms. The selection of particular format for communication depends on the system bandwidth, system's ability to pass DC level information, error checking facility, ease of clock regeneration & synchronizations at receiver, system complexity & cost etc.

The most widely used formats of data representation are given below. There are also available on **ST2106** trainer. Every data format has specific advantages & disadvantages associated with them. We will study one by on see fig 1.

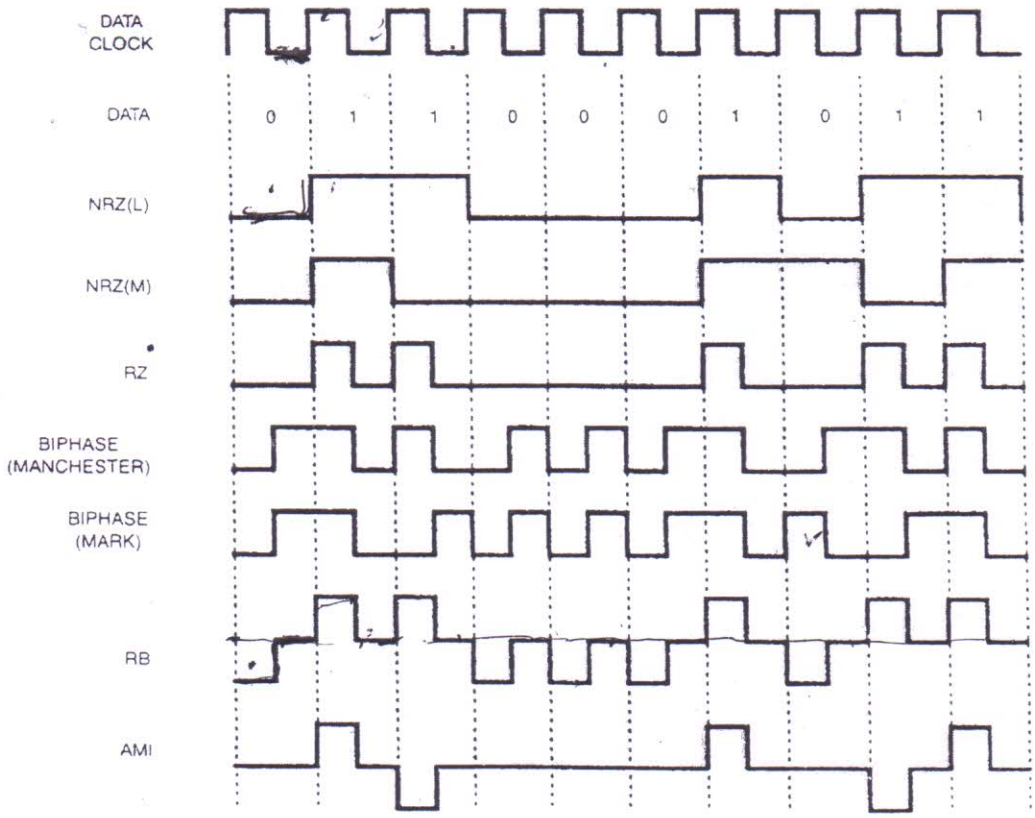


Fig. 1

Non - Return To Zero (Level) NRZ (L) :

It is the simplest form of data representation. The NRZ (L) waveform simply goes low for one bit time to represent a data '0' & high for one bit time to represent a data '1'. Thus the signal alternates only when there is a data change. See fig 2

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Digital Communication Lab: Exp no. 5

TITLE: **DELTA MODULATION (DM)**
OBJECT: a) To study Slope overload distortion.
b)To study Granular or Idel noise.

EQUIPMENTS REQUIRED:

S.NO	APPARATUS NAME	SPECIFICATION
4. 1.	Experimental kit	ST2105
5. 2.	Function generator	1MHZ,SCIENTIFIC
6. 3.	C.R.O.	20MHZ,SCIENTECH

THEORY:

In this system at each sampling time say the K^{th} sampling time, the difference between the sample value at sampling time K and the sample value at the previous sampling time (K-1) is encoded into just a single bit. If signal amplitude has increased, then modulator's output is at logic level 1. If the signal amplitude has increased, the modulator output is at logic level 0.thus the output from the modulator is a series of zeros and ones to indicate rise and fall of the waveform since the previous value.

DELTA MODULATOR WORKS AS FOLLOWS:

The analog signal which is to be encoded into digital data is applied to the +ve input of the voltage comparator which compare it with the signal applied to its –ve input from the integrator output. The comparator's output is logic 0 or 1 depending on weather the input signal at +ve terminal is lower or greater than the –ve terminal input signal. The comparator's output is then latched into a D – flip-flop which is clocked by the transmitter clock. Thus the output of D flip-flop is a latched 1 or 0.synchronous with the transmitter clock edge. This binary data stream is transmitted to receiver & is also fed to the unipolar to bipolar converter. This converts logic zero to voltage level to +4 v & logic 1 to voltage level -4 v. the bipolar output is applied to the integrator whose output is as follows:-

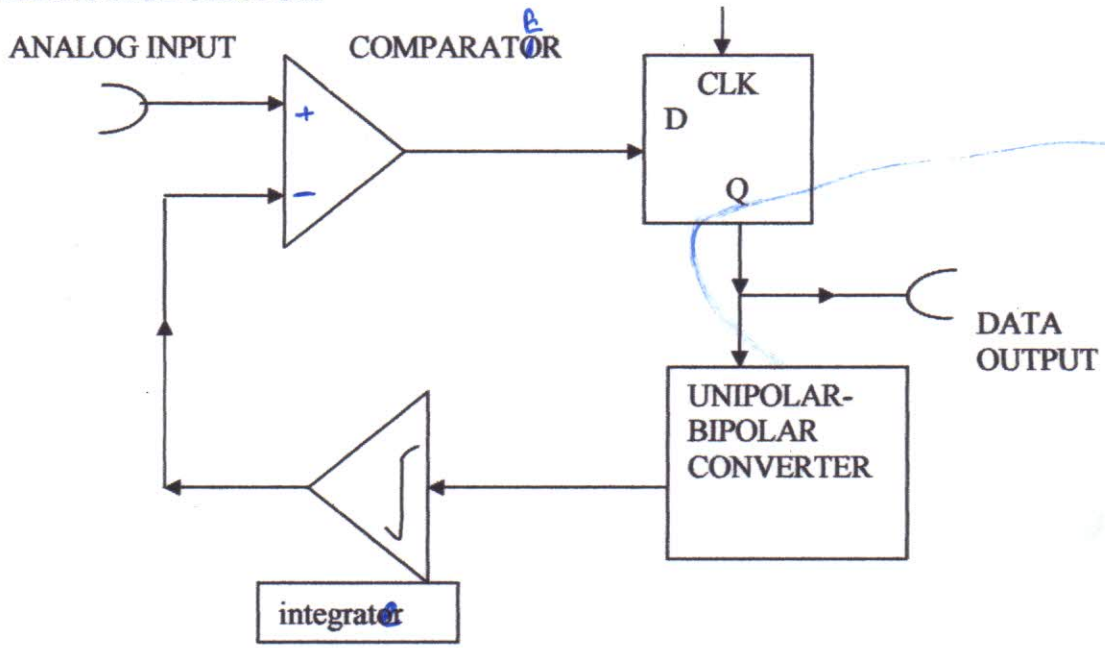
a) Rising linear ramp signal when -4V is applied to it.
b) Falling linear ramp signal when +4V is applied to it.

The integrator O/P is then connected to the –VE terminal of voltage comparator, thus completing the modulator circuit.

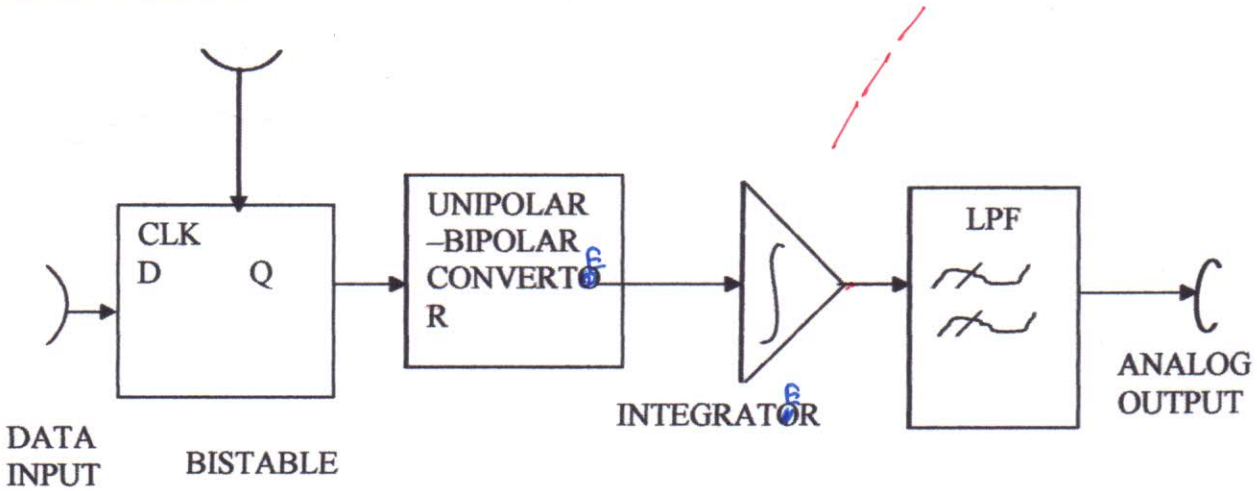
DELTA DEMODULATOR :- The Delta demodulator consist of a D-flip flop, a Unipolar to Bipolar converter followed by an integrator and low-pass filter. The Delta demodulator receives the data from D-Flip-Flop of Delta modulator. It latches this data at every rising edge of **receiver clock which is delayed by half clock period with respect**

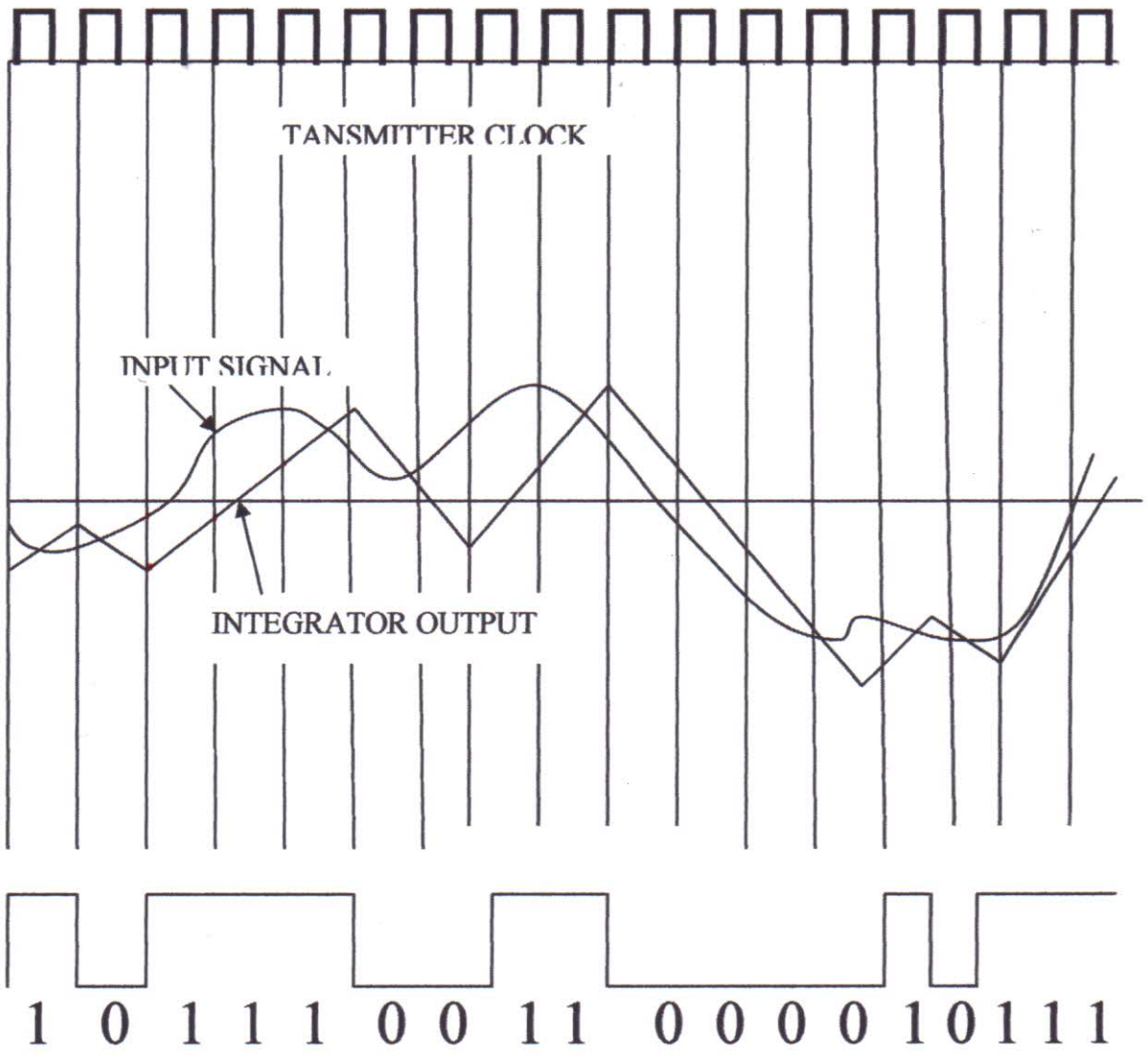
to transmitter clock. This has been done so that the data from transmitter may settle down before being latched into the receiver Flip-Flop.
The Unipolar to Bipolar converter changes the output from D-Flip-Flop to either – 4V or + 4V for logical '1' and '0' respectively.
As it has been seen in case of modulator when the output from unipolar to bipolar converter is applied to integrator, its output tries to follow the analog signal in ramp fashion and hence is a good approximation of the signal itself. The integrator's output contains sharp edges which are 'smoothened out' by the Low – Pass Filter, whose cut-off frequency is just above the audio band.

DELTA MODULATOR



DELTA DEMODULATOR





Let us understand the working of modulator circuit with the analog input waveform applied as above :

Suppose at some time-instance t = 0, the integrator output voltage is lower than the analog input. This causes the voltage comparator voltage to go high i.e. logic '1'. This data is latched than the D-Flip-Flop a the rising edge of transmitter clock., The latched '1' O/P of D-flip flop is translated to -4 V by the Unipolar to Bipolar convertor block. The integrator then ramps up to catch analog signal.

At the next cycle t = 1 the integrator O/P becomes more than the analog I/P so a '0' is latched in to F-flip-flop. The integrator now ramps downward as +4V voltage signal from Unipolar to Bipolar convertor appears at its in put. Thus ramp signal again tries to catch the fallen analog signal.

Thus , after several clock cycle the integrator O/P is approximation of the analog input which tries to catch up the analog input at each sample time. The data stream from D-flip-flop is the Delta Modulators output.

Slope overload distortion :-

This distortion arise because of large dynamic range of the input signal.When the rate of rise of input signal is very high the staircase signal cannot approximate it, the step size become small for staircase signal to follow the input signal. Hence there is a large error between the staircase approximated signal and the original input signal. This error or noise is known slope overload distortion.

Granular Noise :-

Granular noise occurs when the step size is too large compared to small variation in the input signal. This means that for very small variation in the input signal , staircase signal is changed by large amount when the input signal is almost flat, the staircase signal keeps on oscillating by half of the step size around the I/P signal. The error between I/P and approximated signal is called granular noise.

Procedure:- See at last page.

Observation Table:- 1)

Keep In put signal 500 Hz 3 Volts

Sampling freq	% of Distortion

Table 2) :- When Sampling freq is 32 khz and I/P signal voltage is 3 volt

Input signal freq	% of Distortion at Demodulated O/P

Table 3) :- Keep Sampling freq 32 Khz ,I/P Signal freq 2 Khz

In-Put signal Voltage	% of distortion at demodulated O/P

Table No 4) :- Sampling freq 32Khz or 64 Khz and I/P signal 2 Khz

Gain of integrator	% of distortion at demodulated O/P

CONCLUSION :-

Questions:-

1. State two advantages of DM
2. What is slope overload distortion.
3. What is granular noise.
4. State one disadvantage of DM.
5. Which quantization process is used in DM

PROCEDURE TO CARRY OUT EXPERIMENT ON TRAINER KIT ST 2105 :-

(1) Connect the mains supply

(2) Connect the board as shown in the diagram 1

(3) Ensure that the clock frequency selector block switches A & B are in A = 0 and B = 0 position.

(4) Ensure that integrator 1 block's switches are in following position :

(A) Gain control switch in left-hand position (towards switch A & B).

(B) Switches A & B in A=0 and B=0 positions.

(5) Ensure that the switches in integrator 2 block are in following position :

(a) Gain conrol swtich in left-hand position (towards switch A & B)

(b) Switches A & B are in A = 0 and B = 0 positions.

(6) Turn 'ON' of the trainer, see that the power supply LED glows.

(7) In order to ensure for correct operation of the system, we first take the input to 0Vs.

So connect the '+' input of the delta modulator's VOLTAGE COMPARATOR to 0V, and monitor on an Oscilloscope the output of INTEGRATOR 1 (t.p. 17) and the output of the transmitter's LEVEL CHANGER (t.p. 15)

If the Transmitter's LEVEL CHANGER output has equal positive and negative output levels, INTEGRATOR's output will be a triangle wave centred around '0' Volts, as shown in Fig. 5. (Case A). However, if the level changer's negative level is greater than the positive level, the integrator's output will appear as shown in fig 5 (Case B). Should the level changer's positive output level be the greater of the two levels, the integrator's output will resemble that shown in Fig. 5 (Case C).

The relative amplitudes of the level changesr's positive and negative output levels can be varied by adjusting the LEVEL ADJUST present in the BISTABLE AND LEVEL CHANGER CIRCUIT 1 block when it is turned anticlockwise, the negative level increases relative to the positive level, when turned clockwise, the positive level increases relative to the negative.

Prove that you can obtain all the three waveforms shown in fig. 5 by turning the potentiometer from one extreme to another. Try explaining the reason behind it.

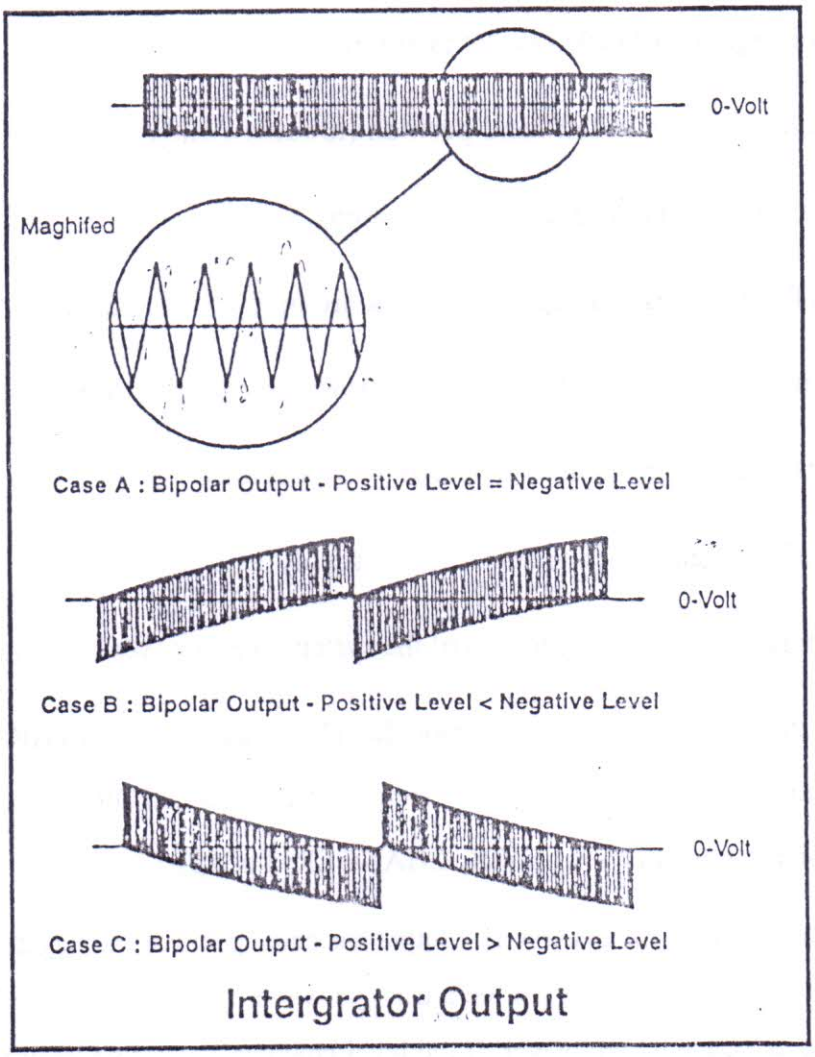


Fig 5

(9) Adjust the transmitter's LEVEL CHANGER preset until the output of INTEgRATOR1 (t.p. 17) is a triangle wave centred around 0 Volts, as shown in fig. 5 (Case A). The peak-to-peak amplitude of the triangle wave at the integrator's output should be 0.5V (approx), this amplitude is known as the **integrator STEP SIZE.**

The output from the Transmitter's BISTABLE Circuit (t.p.14) will now be a stream of alternate '1' and '0' 's'. this is also the output of the delta modulator itself.The Delta Modulator is now said to be 'balanced' for correct operation.

(10) Examine the singnal at the output of INTEGRATOR 2 (t.p. 47) at the receiver. This should be a triangle wave, with step size equal to that of INTEGRATOR 1, and ideally centred around 0 Volts. If there is any DC bias at the output of INTEGRATOR 2, remove it by adjusting the receiver's LEVEL ADJUST preset (in the BISTABLE & LEVEL CHANGER CIRCUIT 2 block). This preset adjusts the relative amplitudes if the positive and negative output levels from the receiver's LEVEL CHANGER circuit only when these levels are balanced will there be no offset at the output of INTEGRATOR 2.

The receiver's LOW PASS FILTER (Whose Cut off frequency is 3.4 KHz.) then filters output the higher - frequency tringle wave, to leave a DC level at the filter's output (t.p. 51). If the receiver's LEVEL ADJUST present has been adjusted correctly, this DC level will be '0' volts, the Delta demodulator is now also balanced for correct operation.

(11) Disconnect the voltage comparator's '+' input from 0V, and reconnect it to the ~ 250Hz output from the FUNCTION GENERATOR block; the modulator's analog input signal is now a 250Hz sinwave.

Monitor this analog signal at the VOLTAGE COMPARATOR'S '+' input t.p. 9 trigger the scope on this signal together with the output of, INTEGRATOR 1 (T.P. 17) Note how the output of the transmitter' integrator follows the analog input, as was illustrated in Fig. 1.

Note :- It may be necessary to readjust slightly the transmitter's LEVEL ADJUST preset (in the BISTABLE & LEVEL CHANGER CIRCUIT 1 block) in order to obtain a stable, repeatable trace of the integrator's output signal.

(12) Display the data of the transmitter's BISTABLE (at t.p. 14), together with the analog input at t.p. 9 (again trigger on this signal), and note that the 250 Hz sincewave has effectively been encoded into a stream of data bits at the bistable's output, ready for transmission to the receiver.

(13) For a full understanding of how the Delta Modulator is working, examine the output of the VOLTAGE COMPARATOR (t.p. 11), the BISTABLE's CLOCK INPUT (t.p. 13), and the LEVEL CHANGER'S BIPOLAR OUTPUT (t.p. 15)

(14) Display the output of INTEGRATOR 1 (t.p. 17) and that of INTEGRATOR 2 (t.p. 47) on the scope. Note that the two signals are very similar in appearance, showing that the demodulator is working as expected.

(15) Display the output of INTEGRATOR 2 (t.p. 47) together with the output of the Receiver's LOW PASS FILTER block (t.p. 51). Note that although the integretor's output has been smoothed out somewhat by the low pass filter, some unwanted 'ripple' still remains at filter's output. This 'ripple' is due to 'quantisation noise' at the integrator's output, which is caused by the relatively large integrator step size.

This step size can be reduced by increasing the rate at which the system is clocked (i.e. the sampling frequency), since this reduces the sampling period, and hence the time available between samples for the integrators to charges up and down.

(16) The current system clock frequency is 32 KHz. This is set by the A,B switches in the CLOCK FREQUENCY SELECTOR block, which are currently in the A = 0, B = 0 positions. While monitoring the same signals, increase the sytem clock frequency to 64KHz, by putting the switches in the A = 0, B = 1 positions.

Note :- If the integrator's output (t.p. 47) no longer gives a stable trace after changing the clock frequency, make a slight adjustment to the transmitter's LEVEL ADJUST

preset (in the BISTABLE & LEVEL CHANGER CICRCUIT 1 block), until the trace is once again stable.

Notice that, at the integrator's (t.p. 47), the frequency of the triangular error signal doubles, and the peak-to-peak amplitude of that error signal (i.e. the step size) is now halved.

Examine the ripple at the low-pass filter's output (t.p. 51). Note that this is now less than it was before.

(17) By changing the system clock frequency to first 128KHz (CLOCK FREQUENCY SELECTOR switches in A=1, B=0 positions), and then to 256KHz (swtiches in A=1, B=0 positions), note the improvement in the low - pass filter's output signal (t.p. 51).

Once again, it may be necessary to adjust slightly the transmitter's LEVEL ADJUST preset, in order to obtain a stable oscilloscope trace.

(18) Using a system clock frequency of 256KHz (which gives a step size of approxmiately 60m V), compare the low pass filter's output. (t.p. 51) with the original analog input (t.p. 9). There should now be no noticeable difference between them, other than a slight delay.

(19) While continuing to monitor the transmitter's analog input (t.p. 9) and the receiver's low-pass filter output (t.p. 51), disconnect the comparator's + input from the 250Hz sinewave output, and reconnect it no the 500Hz, 1KHz and 2KHz outputs in turn. Note that, as the frequency of the analog signal increases, so the low pass filter's output become's more distorted and reduced in amplitude.

(20) In order to understand what has caused this distorion, leave the comparator's + input connected to the 2KHz sinewave output of the Function Generator, and examine the output of INTEGRATOR 2 (t.p. 47). Note that the integrator's output is no longer an approximation to the analog input signal, but is instead somewhat triangular in shape.

Compare this with the output of INTEGRATOR 1 (t.p.17), and note that the two signals are exactly the same; the problem obvisously starts in the Delta Modulator circuit.

(21) Compare the 2KHz analog input signal (t.p. 9) with the output of INTEGRATOR 1 (t.p. 17) it should now become clear what has happended.

The analog signal is now changing so quickly that the integrator's output cannot ramp fast enough to 'catch up' with it, and the result is known as **'slope overloading.'**

(22) Although the system clock frequency i.e. the sampling frequency determines how often the integrator's output direction (up or down) can change, it does not affect how quickly the integrator's output can ramp up and down. Consequently, changing the system clock frequency will not help the slope overload problem; prove this by changing the CLOCK FREQUENCY SELECTOR swtiches, and noting that the problem is still present.

Return the switches to the A=1, B=1 (256KHz clock frequency) position before continuing.

(23) If slope overloading is to be avoided in a practical Delta Modulation system, the transmitter integrator must be able to ramp up or down at a rate which is at least as great as the maximum rate of change at the transmitter's analog input. If the incoming analog signal is a sinewave, its maximum rate of change occurs at the zero crossing point, and is proportiional to both the frequency and the amplitude of the sinewave.

Hence the likelihood of slope overloading can be reduced by either reducing the maximum input frequency, or by reducing the maximum input amplitude to the delta modulator.We have already seen how slope overloading can be avoided by reducing the frequency of the analog input signal since there was no problem with the ~ 250 Hz analog input. Now check that the problem can also be avoided if the amplitude of the input signal is reduced, do this by slowly turning the ~2KHz preset anitclockwise.

Note that there comes a time when the integrator's output can once again follow analog input signal.

(24) Another possible way of overcoming slope overloading is to increase the gain of the integrators so that they can ramp up and down faster, and so follow even those analog input waveforms that change very quickly.

To illustrate this, first return the ~ 2kHz preset to its fully clockwise (maximum amplitude) position, so that slope overloading can once again be seen on the scope.

In each of the two INTEGRATOR blocks, there are two red switches labeled A and B. The 2-bit binary code produced by these switches selects one of four integrator gains, the lowest gain selected when the switches are in the A=0, B=0 positions. For each increasing step in the switch code from A=0, B=0 to A=1, B=1, the integrator gain is doubled.

Change the codes produced by the switches (in both INTEGRATOR 1 and INTEGRATOR 2 blocks) from A=0, B=0 to A = 1, B=1, to double the gain of the two integrators; note that slope overloading still occurs.

Then change both sets of switches to the A=1, B=0 position, and finally to the A=1, B=1, position, to show that slope overloading can be eliminated if the integrator gain is large enough. Once again, it may be necessary to make a slight adjustment to the transmitter's LEVEL ADJUST presed, in order to obtain a stable trace on oscilloscope.

Note that, although it is the gain of INTEGRATOR 1 alone which determines whether or not slope overloading will occur, INTEGRATOR 2 must have the same gain if the amplitude of the Demodulator's analog output is to be equal in amplitude to the Modulator's analog input.

(25) We have observed slope over loading can be covercome by changing any one of the three following options :

(a) reducing the maximum input frequency to the delta modulator.

(b) reducing the maximum input amplitude, or

(c) increasing the integrator gain.

In a practical delta modulation communications system, the signal at the modulator's analog input would normally be in the audio band, so that the maximum input frequency could not be reduced below about 3.4. KHz without losing information. This rules out solution (a) above.

The problem with reducing the amplitude for input signals solution (b) is that smaller input signals then becomes lost in the quantisation noise, they become smaller in amplitude than the integrator's step size.

Finally, if the integrator gain is increased solution (c), much the same problem results as for solution (b), since the larger step size increase quantisation noise and once against 'drowns out' the smaller signals.

In Experiment 2, we will investigate another solution to the problem of slope coverloading which allows us to use high integrator gains for fast-changing analog input signals, and low integrator gains for those smaller signals which would otherwise be 'drowned out'.

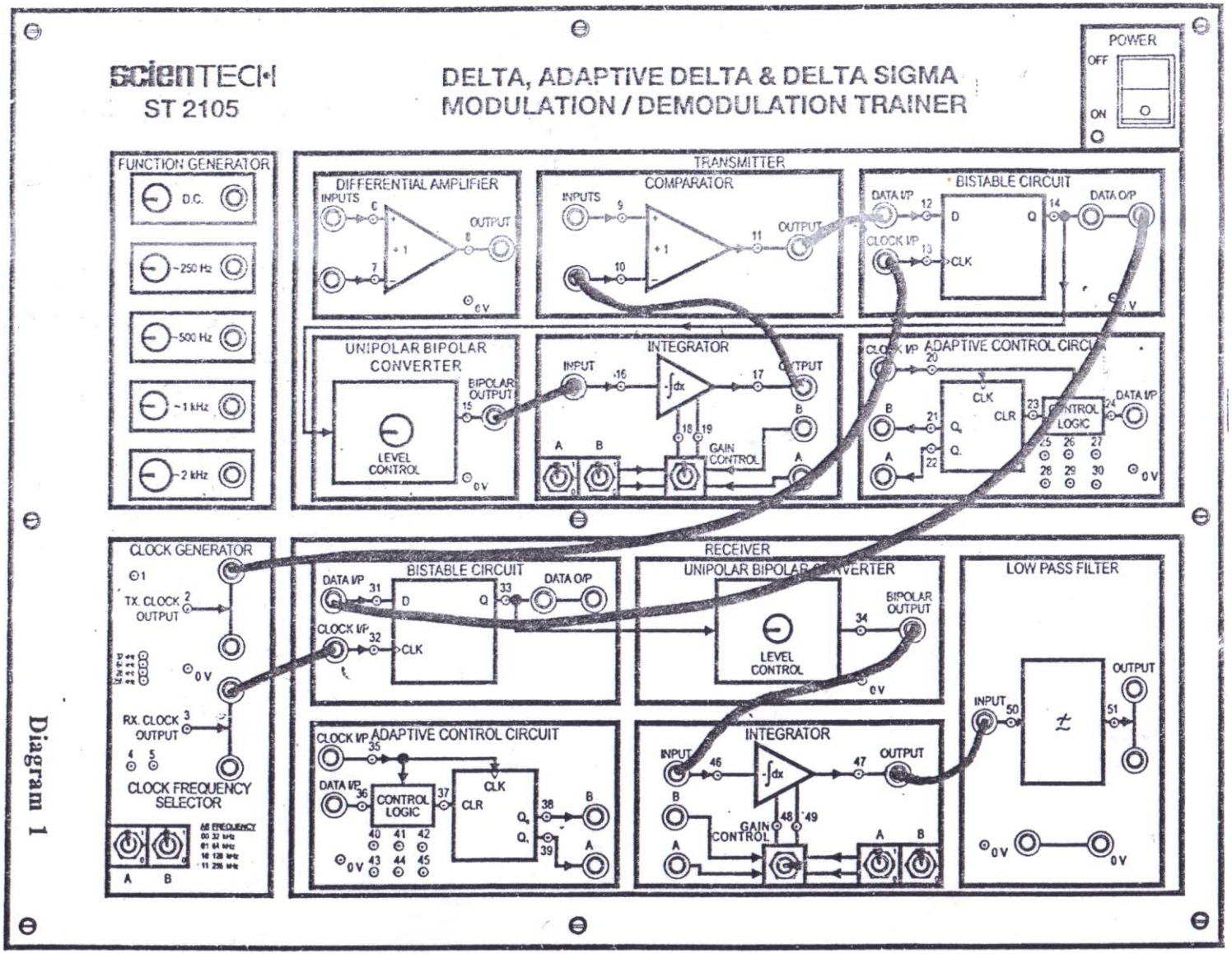

scienTECH
ST 2105
DELTA, ADAPTIVE DELTA & DELTA SIGMA
MODULATION / DEMODULATION TRAINER
POWER
OFF
ON
FUNCTION GENERATOR
D.C.
~250 Hz
~500 Hz
~1 kHz
~2 kHz
TRANSMITTER
DIFFERENTIAL AMPLIFIER
INPUTS
OUTPUT
COMPARATOR
BISTABLE CIRCUIT
DATA I/P
DATA O/P
CLOCK I/P
UNIPOLAR BIPOLAR CONVERTER
BIPOLAR OUTPUT
LEVEL CONTROL
INTEGRATOR
INPUT
GAIN CONTROL
ADAPTIVE CONTROL CIRCUIT
CONTROL LOGIC
CLK
CLR
CLOCK GENERATOR
TX. CLOCK OUTPUT
RX. CLOCK OUTPUT
CLOCK FREQUENCY SELECTOR
RECEIVER
LOW PASS FILTER
0 V

Diagram 1

SILIGURI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Digital Communication Lab: Exp no- 6

TITLE: **ADAPTIVE DELTA MODULATION**
OBJECTIVE:**TO STUDY ADAPTIVE DELTA MODULATION AND DEMODULATION**

EQUIPMENTS REQUIRED:-

S.NO	APPARATUS NAME	SPECIFICATION
10.1.	Experimental kit	ST2105
11. 2.	Function generator	1MHZ,SCIENTIFIC
12. 3.	C.R.O.	20MHZ,SCIENTECH

. **THEORY OF ADAPTIVE DELTA MODULATION:-**
As it has been seen, delta modulation system is unable to chase the rapidly changing information of the analog signal which gives rise to distortion & hence poor quality reception. This is known as slope overloading phenomenon. The problem can be overcome by increasing the integrator gain (i.e. step-size). But using high step-size integrator would lead to a high quantization noise.

QUANSTISATION NOISE:-
It is defined as error introduced between the original signal & the quantized signal due to due to the fixed step size in which the signal (quantized) is incremented. As the error is random in nature & hence unpredictable, it can be treated as noise. High quntisation noise may play havoc on small amplitude signals. The solution to this problem is to increase the integrator gain for fast-changing input & to use normal gain for small amplitude signals.

The basic idea is to increase the integrator gain (it is doubled on this trainer) when slope overload occurs. If still it is unable to catch up with the signal, the integrator gain is doubled again. The integrator on board has four available gains standard, standard X2, standard X4, and standard X8. The integrator thus adopts itself to the gains where its lowest value can just overcome the slope overloading effect.

Functionally, the Adaptive Delta Modulator / Demodulator are shown in fig. 6B & fig. 6C.

As it can be observed, the Adaptive Delta Modulator is similar to the Delta Modulator except for few blocks namely the counter & counter CKT.

The input to to the control circuit is latched data from D Flip-Flop. The counter is reser whenever 'high' appears at the output of the control circuit. Both the counter & the control circuit are clocked by the same TX.CLOCK.

The input to the integrator from the counter is a two bit control word which controls the gain of the integrator. When the output o counter is '00' the gain is lowest (standard) where as it is highest (standard X8) for counters output '11'.

Control word	Integrator Gain
00	Standard
01	Standard X2
10	Standard X4
11	Standard X8

THE WORKING PRINCIPAL OF CONTROL CIRCUIT:-

The control circuit compares the preset data bit from D flip-flop with the previous two data bits. Its output to the counter is high when the three bits are identical, the control circuits output goes low, thus letting the counter advance with every three clock cycles. This advancement continues till the output from the control circuit does not go 'high'. Each time the counter is incremented from 00 integrator gain is doubled till the counter reached '11' where it remains in that state until it is reset by the counter. Similarly, the Adaptive Delta Demodulator is alike Delta Demodulator except for two blocks namely, the control circuit & the counter. They function in the same way as in modulator part, except for the fact that they are clocked by the receiver clock.

Consider the Adaptive Delta Modulator in operation. In normal case, when slope overloading is not occurring, the integrator output always hunt above and below the analog input even after it has caught up with it. The output from the D-flip-flop is a constantly changing '1' to '0' at each TX.CLOCK edge. Even when the analog input is changing at a slightly higher rate, the integrator ramp output is able to catch it in two clock cycles. Thus the output of D-flip-flop is never a three or more consecutive '0' 0r '1's.

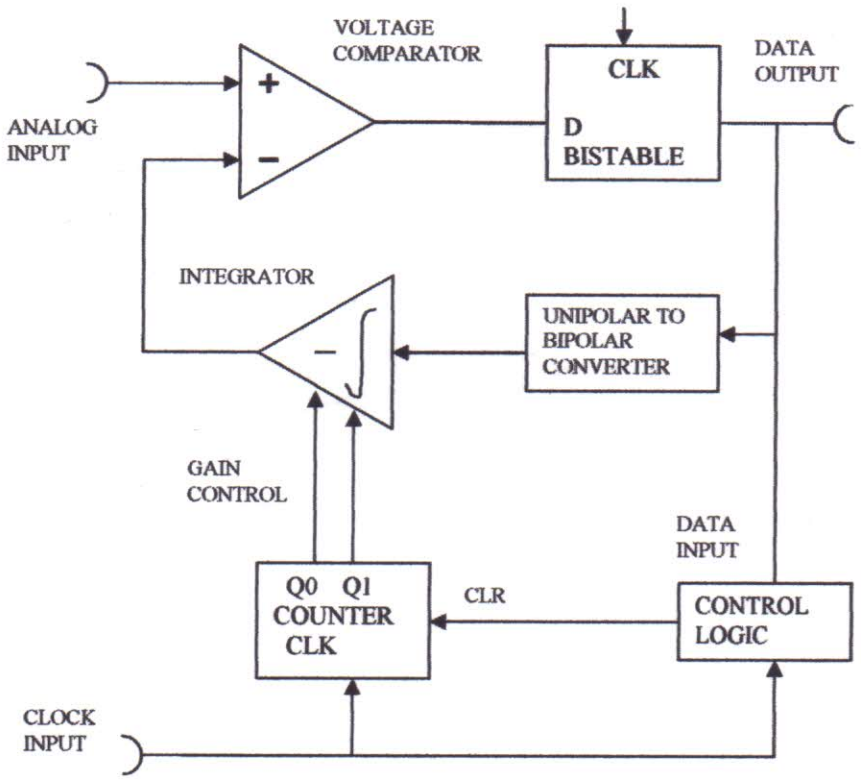
The changing input to the control circuit ensures that its output to the counter is high & hence the counter is always '00' forcing the integrator gain at its lowest value, thereby reducing quantization noise. Here the Adaptive Delta modulator is behaving just as Delta Modulator.

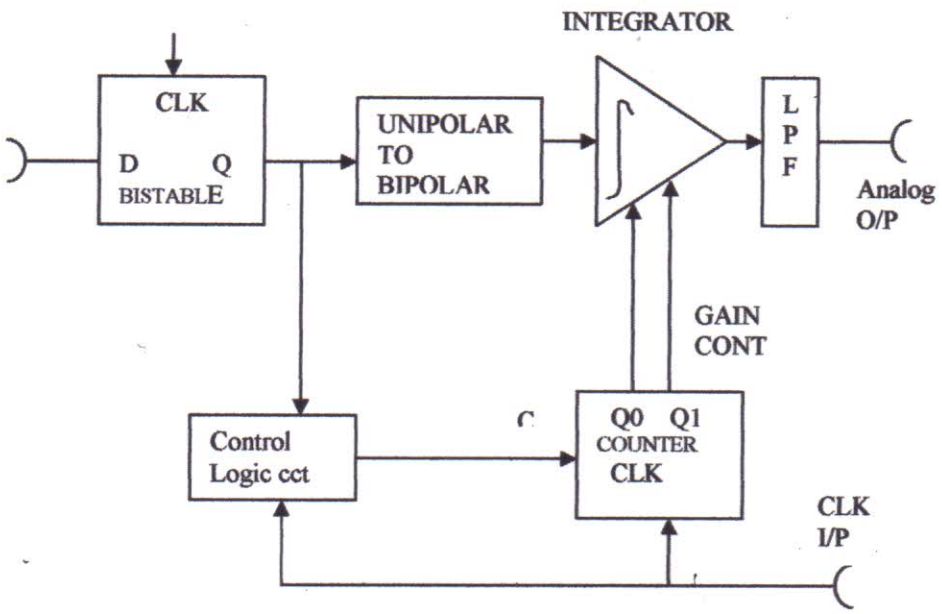
Suppose, now a fast changing analog signal appears at the input of the modulator such that the slope overloading occurs. The integrator output no longer follows the analog signal but it spends its time trying to catch up the analog signal (either it ramps down or up continuously). As a result of continuous ramping in one direction, the D-flip-flops output is either '0' or '1' for three consecutive time. As soon as the third continuous 1/0 is sensed by the control circuit its output goes low. The counter now advance to 01 doubling the integrator gain. This increases the ramping rate of the integrator & it is able to catch the analog signal more faster. In the next clock cycle if the same situation continues the counter advances to '11' where it remains locked until the control logic does not detect a change in the bit level at its input.

As soon as the control circuit detects a change in the bit level, its output goes high, thus restting the counter & thus normalising the integrator gain. In Adaptive Delta Demodulator the control circuit receives the same bit stream as the transmitted one except for the fact that it received after a half clock delay. The functioning of the Receiver's control circuit & counter is same as that of the transmitter's block. Therefore,

excepts for the inherent spikes. The output from integrator is passed to Low Pass Filter to 'smooth out' the waveform. Thus, Adaptive Delta Modulation system is thus able to reduce slop-over load error at an expense of small increase in quanstisation error. It turns out that in matter of speech transmission the reduced slope error provides a net advantage in spite of slight increase in quanstisation error & that the adaptive delta.
Modulator can operate at the bit rate of 32 KB / S with performance comparable to that obtained using PCM at 64 KB /S.

ADAPTIVE DELTA MODULATOR





ADAPTIVE DELTA DEMODULATOR

EXPERIMENT PROCEDURE :- See at last page

OBSERVATION TABLE :- Keep sampling freq at 128 Khz

Input analog Sig (Khz)	Input Sig (Volt)	% of distortion at demodulated O/P in **DM** Mode	% of distortion at demodulated O/P in **ADM** Mode

Questions:-

1. Write one advantage of ADM overDM.
2. What is the purpose of control logic circuit in ADM.
3. Whose SNR is better, DM or ADM, State with reason.
4. Which quantization process is used in ADM.

PROCEDURE TO CARRY OUT THE EXPERIMENT ON TRAINR KIT ST 2165 :-

1. Connect the mains supply.
2. Connect the board as per diagram 2
3. Ensure that the Clock Frequency Selector switches A & B are in A=0 & B=0 position.
4. Ensure that the switches in TX. Integrator gain control block are in following positions :-
   (a) Gain Control switch at the L.N.S. Position.
   (Towards switches A & B)
   (b) Switches A & B in position A=0 & B=0.
5. Ensure that the switches in Receiver's integrator gain control block are in following positions :-
   (a) Gain Control switches at the R.H.S. Position.
   (towards switches A & B)
   (b) Switches A & B in Position A=0 & B=0.
6. Turn all the potentiometers of Function, Generator block namely 250Hz to 2KHz to their fully clockwise positions.
7. Turn ON the power & observe that power supply LED glows.
8. As the Gain Control switch is towards A & B switches the gain setting is still manual, connect the voltage comparator's + VE input to 0V & check whether the modulator & demodulator are balanced for correct operation as in Delta Modulation experimentation.

Change the CLOCK FREQUENCY SELECTOR switches to the A=1, B=1, positions (256kHz Clock Frequency) before continuing.

9. Disconnect the voltage comparator's '+' input from 0V, and reconnect it to the 2KHz output from the FUNCTION GENERATOR block.

10. Monitor the 2KHz analog input at t.p. 9 and the output of INTEGRATOR 1 at t.p. 17. Note that slope overloading is still occuring, as indicated by the fact that the integrator's output is not an approxmiation of the analog input signal.

11. At the transmitter, move the slider of the GAIN CONTROL switch in the INTEGRATOR 1 block to the right-hand position (towards the sockets labeled A,B).

    At the Receiver, move the slider of the GAIN CONTROL switch in the INTEGRATOR 2 block to the left-hand position (again towards the sockets labeled A,B).

    The gain of each integrator is now controlled by the outputs of the counter connected to it. Functionally, the transmitter and receiver are now configured as shown in the fig 6 A & B i.e. as Adaptive Delta Modulator and Demodulator respectively.

12. Once again examine the 2KHz analog input at t.p. 9, and the output of INTEGRATOR 1 at t.p. 17, noting that the slope overloading problem has been eliminated, and that the integrator's output once again follows the analog input signal. Again, it may be necessary to adjust slightly the transmitter's LEVEL ADJUST preset, in order to obtain a stable trace of the integrator's output signal.

13. Comapre the output of INTEGRATOR 1 (t.p. 17) with that of INTEGRATOR 2 (t.p. 47), noting that, as expected, both are identical in appearance.

14. Examine the output of the LOW PASS FILTER (t.p. 51) and the output of INTEGRATOR 2 (t.p. 47). The filter has removed the high-frequency components from the integrator's output signal, to leave a goods, clean 2KHz sinewave.

15. Comapre the origianl 2KHz analog input signal (at t.p. 9) with the output signal from the receiver's LOW PASS FILTER at t.p. 47).

    Note that the Demodulator's output signal is equal in amplitude to the Modulator's input signal, but is delayed somewhat.

16. Disconnect the voltage comaprator's '+' input from the 2 KHz FUNCTION GENERATOR output, and reconnected it in turn to the 1kHz, 500Hz and 250Hz outputs, noting in each case that the Deomodulator's output signal is identicial to the Modulator's input signal, but delayed in time.

17. The Adaptive Delta Modulator / Demodulator system has therefore eliminated any slope overloading problems. To examine in detail how it does this, reconnect the voltage comparator's '+' input to the FUNCTION GENERATOR's 2KHz output, then reduce the system clock (i.e. sampling) frequency to 32 KHz, by putting the CLOCK FREQUENCY SELECTOR switches in the A=0, B=0 positions.

    Although a 32kHz sampling frequency is too low to ensure that an undistored output is obtained from the Demodulator's low pass filter, it does increase the step size to a level which makes it easier to understand how the system is operating.

18. Monitor the 2kHz analog input signal at t.p. 9, and at the output of INTEGRATOR 1 (t.p. 17). It should now become a little clearer as to how the Adptive Delta Modulator is operating. It will be noted that the slope of the integrator's output signal is no longer constant, but increases in a series of discrete steps, in order to 'catch up' with the fast-changing analog input signal.

    If the integrator output does not 'catch up' with the analog input within two clock periods of its direction changing, the slope of the integrator's output signal (i.e.

the integrator gain) is doubled. If it has still not caught up with tha analog input signal by the end of the third clock period, the integrator gain will once again be doubled. If the integrator output still lags behind at the end of the fourth clock period, the integrator's gain is doubled once again, to its maximum value. It then remains at this value untill the integrator output 'catches up' with the analog input signal.Once the integrator's output 'overtakes' the analog input signal, its direction changes, and its rate of change reverts to the minimum value.

(19) Examine also the test points in the ADAPTIVE CONTROL CIRCUIT 1 block (t.p. 20-24), to ensure you have a complete understanding of how the Adaptive Delta Modulator is operating.

(20) While monitoring the outputs of the Modulator's binary counter (t.p.'s 21 and 22), slowly turn the 2kHz preset anticlockwise, in order to reduce the amplitude of the 2kHz analog input signal. Notice that once the analog input signal becomes small enough, both the counter's outputs becomes permanently low, causing the integrator to have minimum gain. This happens because the input signal is now so small that the integrator can always follow it, even with minimum gain.

The result is that small-amplitude input signals can be transmitted with minimum integrator gain, thereby keeping quantisation noise to a minimum at the demodualtor's output.

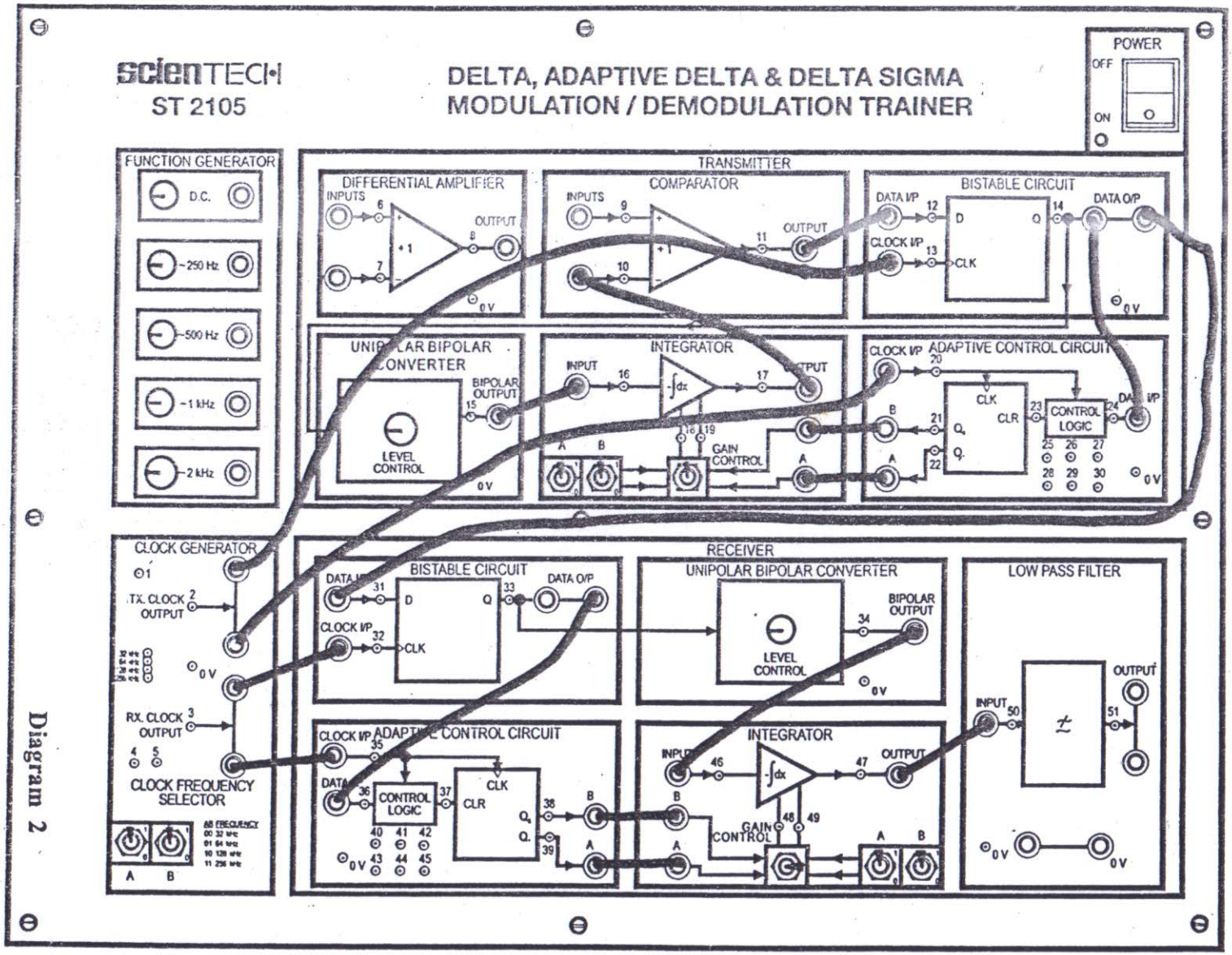

scienTECH
ST 2105
DELTA, ADAPTIVE DELTA & DELTA SIGMA
MODULATION / DEMODULATION TRAINER
POWER
OFF
ON
FUNCTION GENERATOR
D.C.
~250 Hz
~500 Hz
~1 kHz
~2 kHz
TRANSMITTER
DIFFERENTIAL AMPLIFIER
INPUTS
OUTPUT
COMPARATOR
BISTABLE CIRCUIT
DATA I/P
DATA O/P
CLOCK I/P
UNIPOLAR BIPOLAR CONVERTER
BIPOLAR OUTPUT
LEVEL CONTROL
INTEGRATOR
GAIN CONTROL
ADAPTIVE CONTROL CIRCUIT
CONTROL LOGIC
CLOCK GENERATOR
TX. CLOCK OUTPUT
RX. CLOCK OUTPUT
CLOCK FREQUENCY SELECTOR
RECEIVER
LOW PASS FILTER
0V

Diagram 2

SILIGURI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Digital Communication Lab: Exp no. 7

TITLE: **Study of Amplitude Shift Keying Modulation & DemodulationTechniques.**

OBJECTIVE: (i) Observation of the nature and the spectrum of the Modulated Waveform.

(ii) Measurement of the essential bandwidth.
(iii) Analysis of the reception quality by cross co-relation characteristics.
(iv) Measurement of bit error rate in presence of channel noise.

EQUIPMENTS REQUIRED:

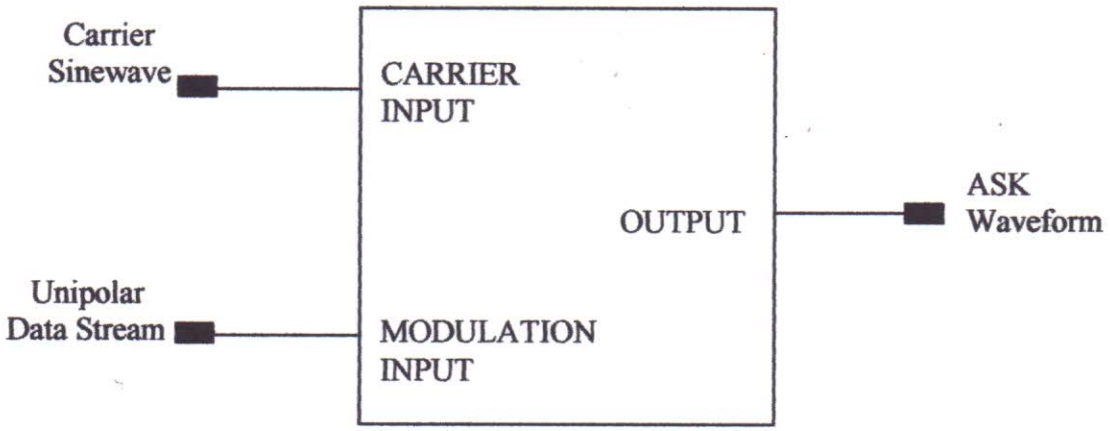
S.NO	APPARATUS NAME	SPECIFICATION
1.	Experimental kit	ST 2103,2104,2106 & 2107.
2.	Function generator	1MHZ,SCIENTIFIC
3.	C.R.O.	20MHZ,SCIENTECH
4.	Spectrum analyzer	3 GigaHZ, GWInstech

THEORY:
The simplest method of modulating a carrier with a data stream is to change the amplitude of the carrier wave every time the data changes. This modulation is known as **Amplitude Shift Keying.**

The simplest way of achieving amplitude shift keying is by switching 'ON' the carrier whenever the data bit is '1' and switching 'OFF'. Whenever the data bit is '0' i.e. the transmitter outputs the carrier for a '1' and totally suppresses the carrier for a '0'. This technique is known as **ON –OFF keying** Fig 20 illustrates the amplitude shift keying for given data stream.

Thus,

DATA = 1 CARRIER TRANSMITTED
DATA = 0 CARRIER SUPPRESSED



Double – Balanced
Modulator

ASK MODULATION

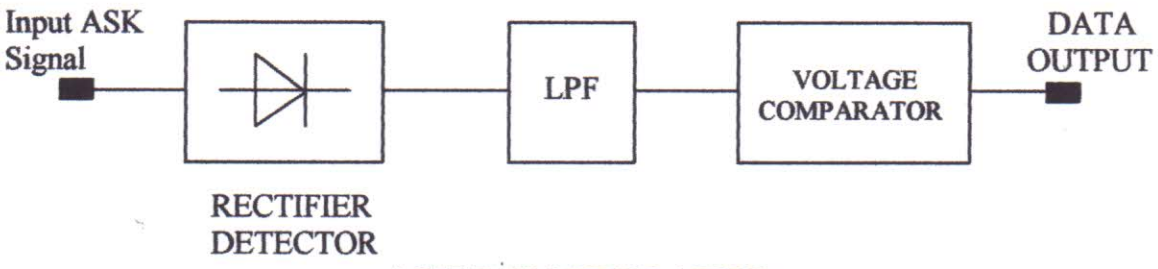
The ASK waveform is generated by a balanced modulator circuit, also known as a **linear multiplier.** As the name suggests, the device multiplies the instantaneous signal at its two inputs. The output voltage being product of the two input voltages at any instance of time. One of the inputs is a.c. coupled 'carrier' wave of high frequency. Generally, the carrier waved is a sinewave since any other waveform would increase the bandwidth, without providing any advantages. The other input which is the information signal to be transmitted, is d.c. coupled. It is known as **modulating signal.**

In order to generate ASK waveform it is necessary to apply a sine wave at carrier input and the digital data stream at modulation input. The **double – balanced modulator** is shown in above figure.
The data stream applied is unipolar i.e. 0 volts at logic '0' and +5 Volts at logic '1'. The output of balanced modulator is a sinewave, unchanged in phase when a data bit '1' is applied to it. In this case the carrier is multiplied with a positive constant voltage when the data bit '0' is applied, the carrier is multiplied by 0 volts, giving rise to 0 volt signal at modulator's output.
The ASK modulation result in a great simplicity at the receiver. The method to demodulate the ASK modulation results in a great simplicity at the receiver. The method to demodulate the ASK waveform is to rectify it, pass it through the filter and 'Square Up' the resulting waveform. The output is the original data stream.

The various steps involved are summed below

Step A: The ASK waveform is **rectified by a diode** rectifier, giving a positive going signal. This signal is too rounded to be used as digital data. Also the carrier component is still present and it is of unreliable amplitude due to the attenuation and noise in transmission path. In fact it is a great drawback associated with ASK modulation. The data level may be misinterpreted by the receiver if the amplitude change is too much.

Step B: After rectification, the signal is **passed through the low pass filter** to remove the carrier component. This result in a slightly rounded pulse of unreliable amplitude.



ASK DEMODULATOR

Step C: These rounded pulsed are then **'Squared Up' (i.e. shaped in a square wave fashion) by passing it through** voltage comparator set at a threshold level. If the input voltage exceeds the threshold level, the comparator output is a +5V signal and in other case it is 0V. Thus at the end we have the true copy of the original input data .

Amplitude shift keying is fairly simple to implement in practice, but it is less efficient, because the noise inherent in the transmission channel can deteriorate the signal so much that the amplitude changes in the modulated carrier wave due to noise addition, may lead to the incorrect decoding at the receiver. This is particularly true when the noise added is comparable to the comparator threshold level. Hence, **this technique is not widely used is practice.** Application wise, it is however used in diverse areas and old as emergency radio transmissions and fiber-optic communications.

Procedure: See at the last page

Observation :- i) Observe and plot the input Data and modulated signal wave form with a CRO.
ii) Observe and plot the demodulated Data at the Output.
iii)Observe the power spectrul density of modulated signal with a spectrum analyzer.
v) Apply a sinosidal signal as input and measure the % of distortion of the demodulated signal.

I/P Signal Freq	I/P Signal Amplitude	Demodulated signal Amp	% of distortion

Conclusion:

Questions :

1. What is the need of carrier modulation
2. Define Amplitude Shift Keying
3. What is the main disadvantage of ASK
4. Draw the power spectral density of ASK signal

(1) The experiment makes use of four trainers namely **ST2103, ST2104, ST2106 & ST2107.** **ST2103** TDM Pulse Code Modulation Transmitter Trainer serves as a data source while ST2104 TDM Pulse Code Modulation Receiver Trainer serves as analog signal recoverer. ST2106 serves as data formatting (Conditioning) device while ST2107 reformats (decondition) the data.

ST2103 & ST2106 Trainers serves as transmitter for our system & ST2107 & ST2104 Trainer serves as receiver.

(2) Ensure that all trainers are switched OFF, until the complete connection are made.

(3) Check ST2104 Trainer's CLOCK REGENERATION CIRCUIT Set up for correct operation as given in experimentation 1 of ST2103 / 4 work book

(4) Set up the following conditions on ST2103 trainer

(A) **MODE** switch set in **FAST** position.

(B) **PSEUDO - RANDOM SYNC CODE GENERATOR** switched **'ON'.**

(C) **ERROR CHECK CODE SELECTOR** switches **A & B in A=0 & B=0 Positions.**

(D) All switched faults 'OFF'

(5) Set ST2106 trainer's MODE switch in position ' 1 '

(6) Set up following conditions on ST2104 trainers :

(A) **MODE** switch set in **FAST** position

(B) **PSEUDO - RANDOM SYNC CODE DETECTOR IN 'ON'** position.

(C) **ERROR CHECK CODE SELECTOR** switch A & B IN A = 0 & B = 0 position.

(D) All switched faults kept 'OFF'

(7) Make the following connections between ST2103 A, ST2106 trainers.

ST2103 Trainer **ST2106 Trainer**

(A) TX CLOCK OUTPUT (t.p. 3) TO TX .CLOCK INPUT

(B) PCM OUTPUT (t.p. 44) TO TX .DATA INPUT

(8) Connect the TX TO OUTPUT (t.p 4) on ST2103 trainer to external trigger input of the oscilloscope. Set to negative edge triggered mode in oscilloscope. It may be necessary to adjust the trigger level manually to obtain a stable waveform.

(9) On ST2103 trainer make following connections :

(A) DC 1 to CH 0 INPUT

(B) CH 0 input to CH 1 input

This is done to supply the same voltage level to each of the two time division multiplexed channels. Thus we are able to get the same data stream for any time frame.

(10) Make the rest of the connections as shown in configuration Fig 3.

(11) Switch 'ON' the power

(12) On ST2103 trainer adjust the D.C.1 potentiometer until the 7 bit code displayed on A / D CONVERTER LED's is

D6	D5	D4	D3	D2	D1	DO
0	1	0	0	0	1	1

(13) Observe the DATA CLOCK output at t.p 4 on ST2106 trainer's DATA FORMAT block with oscilloscope. Adjust the oscilloscopes time base & position control until each rising edge of data clock coincides with one of scope's. vertical graticule line as shown in **Figure 4.** Each main division on scope's horizontal axis now represent one data bit time. Adjust the trigger level (manually, if necessary, to obtain a stable trace.) This sets convenient reference against which to observe the other wave forms.

1. Also Set PULSE GENERATOR DELAY ADJUST fully Clockwise in step 6.

(14) Switch OFF the power. Connect additional the board as shown in Fig.24 as follows :

(A) On ST2106 trainer :

(i) NRZ (L) Output (t.p.5) to Carrier Modulation Circuits Modulation Input. (t.p.27).

(ii) 1.44 MHz carrier output (t.p.16) to carrier input socket of modulator Ckt (t.p.26).

(B) Between ST2106 and ST2107 :

Modulator 1 output (t.p.28) to ASK Demodulator input (t.p.21).

(C) On ST2106 and ST2107 :

(i) ASK Demodulator output (t.p.22) to L.P.Filter 1 input (t.p.23).

(ii) L.P.Filter 1 output (t.p.24) to comparator 1 input (t.p.46)

(D) On ST2104 trainer

(i) PCM. DATA INPUT (t.p.1) to Clock Regen. Circuit input (t.p.3)

(ii) Clock Regn Circuit output t.p.8 to RX.CLOCK input (t.p.46)

(E) Connect Comparator 1 output (t.p.47) on ST2107 to PCM DATA INPUT (t.p.1) on ST2104

(15) Turn ON the trainers : Monitor NRZ (L) output (t.p.5) from ST2106 trainer on one channel of the oscilloscope Use the other channel to monitor the output of modulator 1 (t.p.28) in ST2106 trainer.

(16) Three variables have been provided in the modulators block. Their use may be necessary to obtain a required ASK waveform. These variables are

(A) **GAIN :** This pot. adjust the amplification of the modulator's output. Adjust this pot. till the output is not a 2Vpp signal in 'ON' state.

(B) **MODULATION OFFSET :** This control is used to adjust the amplitude of the 'off signal. Adjust this control till the amplitude of the 'off' signal is an close to zero as possible.

(C) **CARRIER OFFSET :** This control adjusts the off bias level of the ASK waveform. Adjust this control till the 'off' level occurs midway between the 'ON' signal peaks.

(17) To see the demodulation process, observe the output at the ASK demodulator (t.p.22) & low pass filter (t.p.24) on ST2107 trainer.

(18) The last stage of demodulation is 'squaring up' of filter output. In order to achieve this it is necessary to adjust the BIAS level for comparator 1 so that the output has the correct pulse width.

Adjust it till the output signal pulse width is not similar to the NRZ (L) data pulse width. You can observe these two simulaneously on the dual trace oscilloscope. The two will be identical once the BIAS level is adjusted except for short delay between them.

(19) Turn 'ON' the Pseudo-Random Sync Code Generator on ST2103 trainer. This pulls the Transmitter & Receiver in 'Frame - Synchronisation'. Observe the A/D Converter L.E.D.'s on ST2103 trainer & D/A Converter L.E.D.s on ST2104 trainer. Now they will be carrying the same data. Change the position of the D.C.1 pot observe that the same change is refelcted at the receiver.

(20) **Turn 'OFF' the power :** Disconnect CH.0 & CH.1. Instead connect them to 1KHz & 2KHz signal respectively. Turn ON the trainers. & Check the reconstructed analog output on ST2104 CH.0 & CH.1 (t.p.33 & 36).

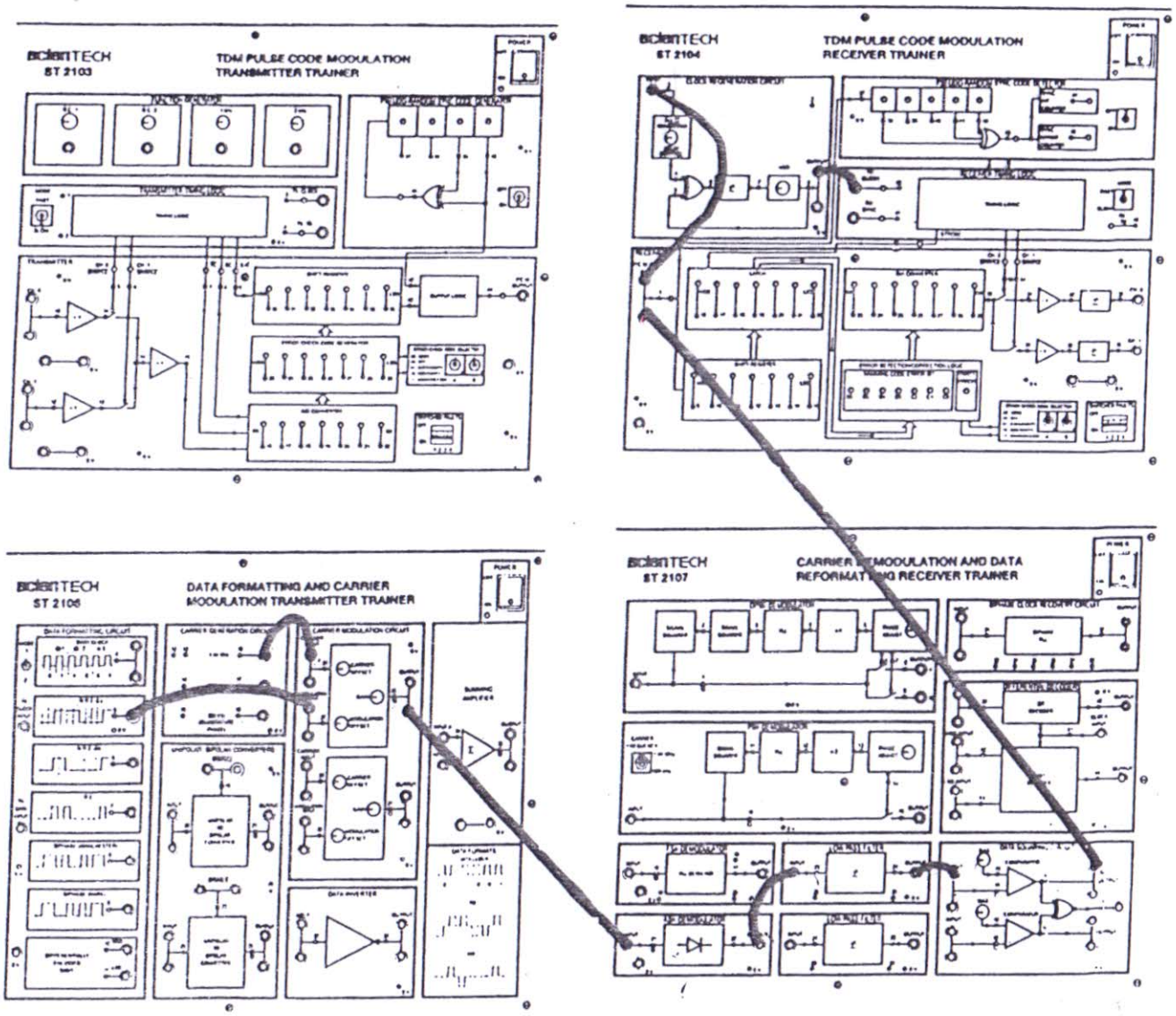

scientech
ST 2103
TDM PULSE CODE MODULATION
TRANSMITTER TRAINER
scientech
ST 2104
TDM PULSE CODE MODULATION
RECEIVER TRAINER
scientech
ST 2106
DATA FORMATTING AND CARRIER
MODULATION TRANSMITTER TRAINER
scientech
ST 2107
CARRIER DEMODULATION AND DATA

Fig. 24

SILIGURI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Digital Communication Lab: Exp no. 8

TITLE: **TO STUDY FREQUENCY SHIFT KEY MODULATION AND DEMODULATION**

OBJECTIVE: (i) Observation of the nature and the spectrum of the Modulated Waveform.

(ii) Measurement of the essential bandwidth.
(iii) Analysis of the reception quality by cross co-relation characteristics.
(iv) Measurement of bit error rate in presence of channel noise.

EQUIPMENTS REQUIRED:

S.NO	APPARATUS NAME	SPECIFICATION
1.	Experimental kit	ST 2103,2104,2106& 2107.
2.	Function generator	1MHZ,SCIENTIFIC
3.	C.R.O.	20MHZ,SCIENTECH
4.	Spectrum analyzer	3 GigaHZ, GWInstech

Theory:

In frequency shift keying, the carrier frequency is shifted in steps (i.e. from one frequency to another) corresponding to the digital modulation signal. If the higher frequency is used to represent a data '1' and lower frequency a data '0', the resulting Frequency shift keying waveform appears.

Thus,

DATA = 1 HIGH FREQUENCY
DATA = 0 LOW FREQUENCY

On a closer look at the FSK waveform, it can be seen that it can be represented as the sum of two ASK waveforms.

Let us assume that we apply the above data stream to an ASK modulator using the higher frequency carrier.

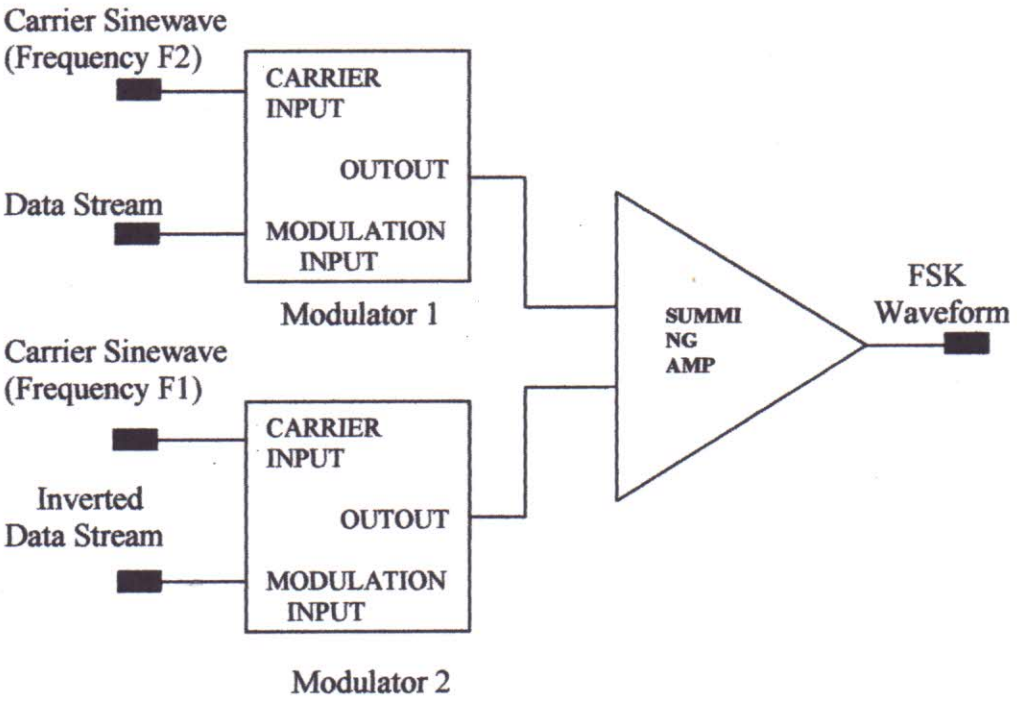
Let us now invert the original data stream.

Original Data Stream	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**1**
Inverted Data Stream	1	0	0	1	1	1	0	1	0	0

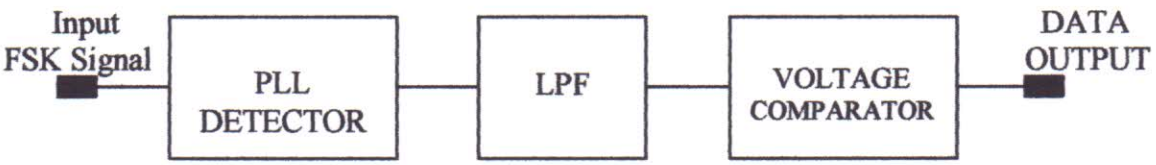
We now apply the inverted data stream to the ASK modulator using a lower stream frequency carrier. The result is the original data '0' filled with the lower frequency carrier.

Lastly, we have to sum the two ASK waveform, to get a FSK wave.

The functional blocks required in order to generate the FSK signal. The two carriers have different frequencies and the digital data is inverted in one case.



The demodulation of FSK waveform can be carried out by a Phase Locked Loop. As known, the phase locked loop tries to 'lock' to the input frequency. It achieves this by6 generating corresponding output voltage to be fed to the voltage controlled oscillator, if any frequency deviation at its input is encountered. Thus the PLL detector follows the frequency changes and generates proportional output voltage. The output voltage from PLL contains the carrier components. Therefore the signal is passed through the low pass filter to remove them. The resulting wave is too rounded to be used for digital data processing. Also, the amplitude level may be very low due to channel attenuation. The signal is 'Squared Up' by feeding it to the voltage comparator.



Since the amplitude change in FSK waveform does not matter, this modulation technique is very reliable even in noisy and fading channels. But there is always a price to be paid to gain that advantage.

The price in this case is widening of the required bandwidth. The bandwidth increase depends upon the two carrier frequencies used and the digital data rate. Also, for a given data, the higher the frequencies and the more they differ from each other, the wider the required bandwidth. The bandwidth required is at least doubled than that in the ASK modulation. This means that lesser number of communication channels for given band of frequencies.

Procedure: See at the last page

Observation :- i) Observe and plot the input Data and modulated signal wave form with a CRO.
ii) Observe and plot the demodulated Data at the Output.
iii)Observe the power spectrul density of modulated signal with a spectrum analyzer.
v) Apply a sinosidal signal as input and measure the % of distortion of the demodulated signal.

I/P Signal Freq	I/P Signal Amplitude	Demodulated signal Amp	% of distortion

Conclusion:

Questions.

1. Draw the block diagram for FSK generation
2. Draw Power Spectral density of FSK signal
3. What type receiver is mainly used for FSK system
4. Write the bandwidth expression of FSK signal

(1) The experiment makes use of four trainers namely **ST2103, ST2104, ST2106 & ST2107.** **ST2103** TDM Pulse Code Modulation Transmitter Trainer serves as a data source while ST2104 TDM Pulse Code Modulation Receiver Trainer serves as analog signal recoverer. ST2106 serves as data formatting (Conditioning) device while ST2107 reformats (decondition) the data.

ST2103 & ST2106 Trainers serves as transmitter for our system & ST2107 & ST2104 Trainer serves as receiver.

(2) Ensure that all trainers are switched OFF, until the complete connection are made.

(3) Check ST2104 Trainer's CLOCK REGENERATION CIRCUIT Set up for correct operation as given in experimentation 1 of ST2103 / 4 work book

(4) Set up the following conditions on ST2103 trainer

(A) **MODE** switch set in **FAST** position.

(B) **PSEUDO - RANDOM SYNC CODE GENERATOR** switched **'ON'.**

(C) **ERROR CHECK CODE SELECTOR** switches **A & B in A=0 & B=0 Positions.**

(D) All switched faults 'OFF'

(5) Set ST2106 trainer's MODE switch in position ' 1 '

(6) Set up following conditions on ST2104 trainers :

(A) **MODE** switch set in **FAST** position

(B) **PSEUDO - RANDOM SYNC CODE DETECTOR IN 'ON'** position.

(C) **ERROR CHECK CODE SELECTOR** switch A & B IN A = 0 & B = 0 position.

(D) All switched faults kept 'OFF'

(7) Make the following connections between ST2103 A, ST2106 trainers.

ST2103 Trainer **ST2106 Trainer**

(A) TX CLOCK OUTPUT (t.p. 3) TO TX .CLOCK INPUT

(B) PCM OUTPUT (t.p. 44) TO TX .DATA INPUT

(8) Connect the TX TO OUTPUT (t.p 4) on ST2103 trainer to external trigger input of the oscilloscope. Set to negative edge triggered mode in oscilloscope. It may be necessary to adjust the trigger level manually to obtain a stable waveform.

(9) On ST2103 trainer make following connections :

(A) DC 1 to CH 0 INPUT

(B) CH 0 input to CH 1 input

This is done to supply the same voltage level to each of the two time division multiplexed channels. Thus we are able to get the same data stream for any time frame.

(10) Make the rest of the connections as shown in configuration Fig 3.

(11) Switch 'ON' the power

(12) On ST2103 trainer adjust the D.C.1 potentiometer until the 7 bit code displayed on A / D CONVERTER LED's is

D6	D5	D4	D3	D2	D1	DO
0	1	0	0	0	1	1

(13) Observe the DATA CLOCK output at t.p 4 on ST2106 trainer's DATA FORMAT block with oscilloscope. Adjust the oscilloscopes time base & position control until each rising edge of data clock coincides with one of scope's. vertical graticule line as shown in **Figure 4.** Each main division on scope's horizontal axis now represent one data bit time. Adjust the trigger level (manually, if necessary, to obtain a stable trace.) This sets convenient reference against which to observe the other wave forms.

(14) Switch OFF the power. Make the additional **connections as shown in Fig. 31 as follows :**

(A) On ST2106 Trainer :

(i) NRZ (L) output (t.p.5) to modulation input of unipolar-Bipolar converter (t.p. 27)

(ii) Modulation input (t.p.27) to data inverter input (t.p.32)

(iii) Modulator output (t.p.28) to summing amplifier input A (t.p.34)

(iv) Data inverter output (t.p.33) to modulation input of modulator 2 (t.p.30)

(v) 1.44 MHz carrier (t.p.16) to Modulator 1 carrier input (t.p.26)

(vi) 960KHz (I) carrier (t.p.17) to modulator 2 carrier input (t.p.29)

(vii) Modulator 2 output (t.p.31) to summing amplifier input (t.p.35)

(B) Between ST2106 & ST2107 trainer :

(i) Summing amplifier output (t.p.36) to PLL detector input (t.p.16)

(C) On ST2107 trainer :

(i) PLL Detector ouput (t.p.17) to Low Pass Filter 1 input (t.p.23)

(ii) Low Pass Filter 1 Output (t.p.24) comparator 1 input (t.p.46)

(D) Between ST2107 & ST2104 trainer :

(i) Comparator 1 Output (t.p.24) to PCM. DATA INPUT (t.p.1)

FSK

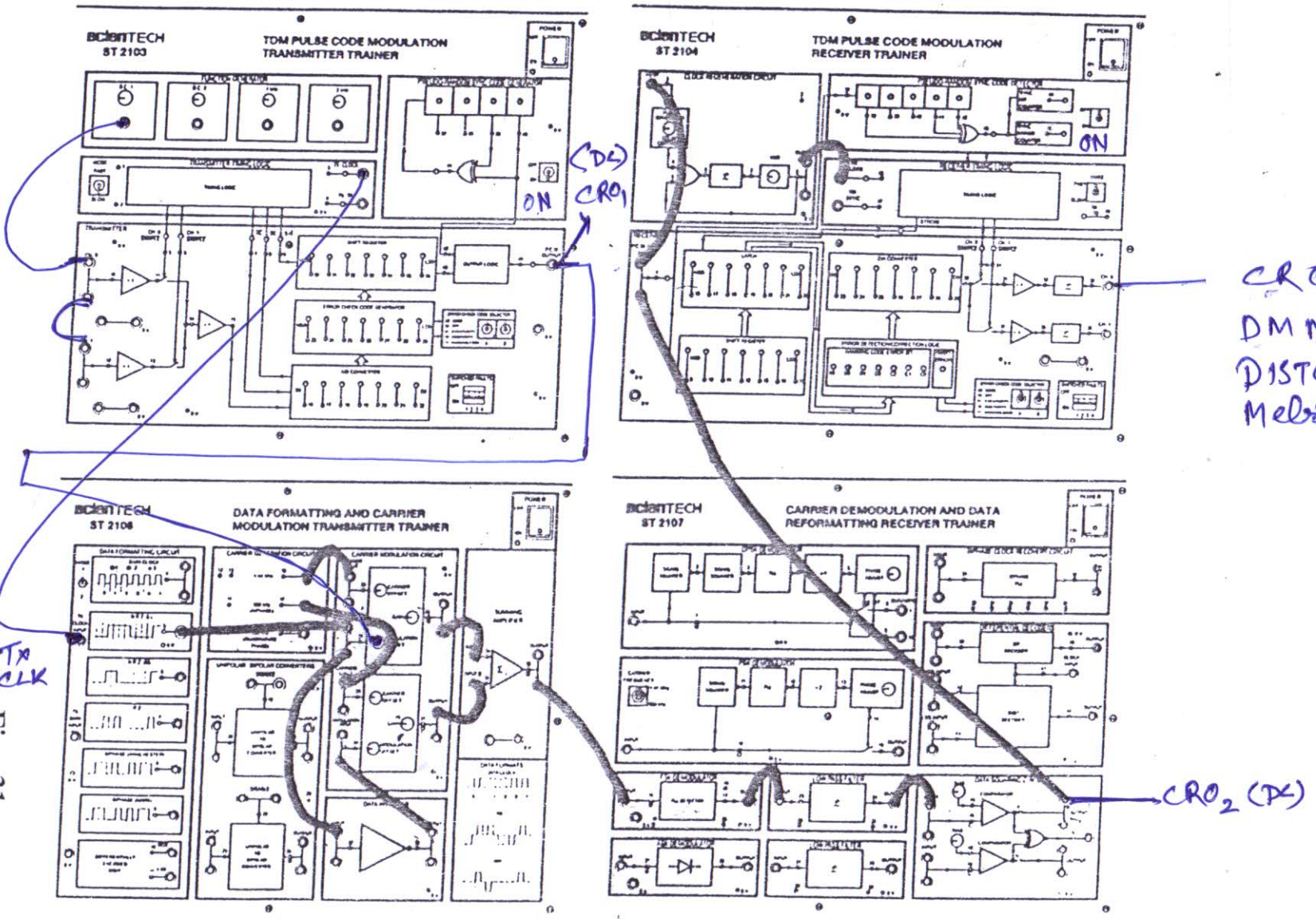

ScienTECH
ST 2103
TDM PULSE CODE MODULATION
TRANSMITTER TRAINER
ScienTECH
ST 2104
TDM PULSE CODE MODULATION
RECEIVER TRAINER
ON
ON
(DC)
CRO1
CRO (AC)
DMM (DC)
DISTORTION
Meter (AC)
ScienTECH
ST 2106
DATA FORMATTING AND CARRIER
MODULATION TRANSMITTER TRAINER
ScienTECH
ST 2107
CARRIER DEMODULATION AND DATA
REFORMATTING RECEIVER TRAINER
TX CLK
CRO2 (DC)

Fig. 31

(E) **On ST2104 trainer :**

(i) PCM . DATA Input (t.p.1) to Clock Regeneration Circuit Input (t.p.3)

(ii) Clock Regeneration Circuit Output (t.p.8) to RX.CLOCK Input (t.p.46)

(15) Monitor the output of modulator 1 (t.p.28) on ST2106 trainer. Make the adjustments of the given controls in the modulator block as follows :-

(A) **GAIN :** Adjust this pot untill the amplitude of the 'ON' signal is 2 Vpp.

(B) **MODULATION OFF SET :** It is used to control the amplitude of off signal. Adjust it till the 'OFF' signal level doesn't approach as close to zero as possible.

(C) **CARRIER OFF SET :** This adjusts the 'OFF' bias level of the ASK waveform. Adjust this control until the 'OFF' level occurs midway between the peaks of the 'ON' level of the signal

(16) Repeat step no 15 with modulator 2 by observing its output at t.p.31.

(17) Observe the output of the summing amplifier on the ST2106 trainer at (t.p.36) Note that it is the FSK waveform for the given data.

Adjust the 'GAIN' control of Modulator 2, if necessary to make the amplitude the two frequency components equal.

(18) Display the FSK waveform simultaneously with NRZ(L) output. Observe that for data bit '0' the FSK signal is at lower frequency (960KHz) & for data bit '1', the FSK signal is at higher frequency (1.44 MHz).

(19) Now, to study about demodulation, examine the input (t.p.16) and the output (t.p.17) of ST2107 FSK Demodulator. The PLL detector has been used as the FSK demodulator on this trainer.

Observe that the output voltage of the PLL detector is greater for higher incoming frequency. Also, observe that for both incoming carrier frequencies, the demodulator's output also contains a component at that frequency.

(20) The unwanted frequency component is removed by passing it through the low pass filter. On a dual trace oscilloscope examine the input (t.p.23) & output (t.p.24) of ST2107 Low Pass Filter 1 simiultaneously. Observe that the output contains no carrier frequency components.

(21) The rounded output of the low pass filter is removed by passing it through the Data Squaring Circuit. But prior to it, the BIAS level of the comparator 1 is to be adjusted to a value until the output pulse width (t.p.47) is same as the NRZ (L) input (t.p.5) on ST2106. For this purpose, display them simultaneously. Observe that the comparator output is slightly delayed then NRZ (L) input.

(22) Turn ON the PSEUDO-RANDOM SYNC GENERATOR. This locks the transmitter & receiver in 'frame synchronisation' Therefore the data on A/D CONVERTER L.E.D.'s on ST2103 trainer is same as that present on D/A CONVERTER L.E.D.'s on ST2104 trainer. You can examine this fact by varying the data on transmitter trainer ST2103 by the D.C.1 pot. variation.

(23) To examine FSK modulation & demodulation for a time variant data/wave, connect CH.0 and CH.1 input to ~1KHz & ~2KHz function generator outputs instead of D.C.1./D.C.2 Input.

Remember to Connect/Disconnect the links only with the trainers in SWITCHED OFF position Switch the oscilloscope for internal triggering. Check the reconstructed waveform CH.0 & CH.1 outputs on ST2104 trainer. They should be identical to the input waveforms. Remember, the two outputs are independent of each other & thus interference free. Any interference if present can be removed by adjusting PHASE GENERATOR DELAY ADJUST CONTROL.

(24) You can try experimenting FSK modulation / demodulation by using any other data format. Equally, any of the other binary outputs from the Data Formatting Circuits can be used. But remember to reformat it to NRZ (L) waveform on ST2107 board, after demodulation, before feeding it to the ST2104 trainer.

SILIGURI INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Digital Communication Lab: Exp no. 9

TITLE: **TO STUDY PHASE SHIFT KEY MODULATION AND DEMODULATION**

OBJECTIVE: (i) Observation of the nature and the spectrum of the Modulated Waveform.

(ii) Measurement of the essential bandwidth.
(iii) Analysis of the reception quality by cross co-relation characteristics.
(iv) Measurement of bit error rate in presence of channel noise.

EQUIPMENTS REQUIRED:

S.NO	APPARATUS NAME	SPECIFICATION
1.	Experimental kit	ST 2103,2104,2106& 2107.
2.	Function generator	1MHZ,SCIENTIFIC
3.	C.R.O.	20MHZ,SCIENTECH
4.	Spectrum analyzer	3 GigaHZ, GWInstech

Theory: Phase shift Keying involve the phase change of the carrier sine wave between **0°** and **180°** in according with the data stream to be transmitted.

Functionally, the PSK modulator is very similar to the ASK modulator. Both uses balanced modulator to multiply the carrier with the modulating signal. But in contrast to ASK technique, the digital signal applied to the modulation input for PSK generation is bipolar i.e have equal positive and negative levels. When the modulating input is positive the output of modulator is a sine wave in phase with the carrier input. Where as for negative voltage levels, the output of the modulator is a sine wave which is shifted out of phase by 180° from the carrier input. This happen because the carrier input is now multiplied by the negative constant level. Thus the output in phase when a change in polarity of the modulating signal results.

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EQUIPMENTS REQUIRED:

S.NO	APPARATUS NAME	SPECIFICATION
1.	Experimental kit	ST 2103,2104,2106& 2107.
2.	Function generator	1MHZ,SCIENTIFIC
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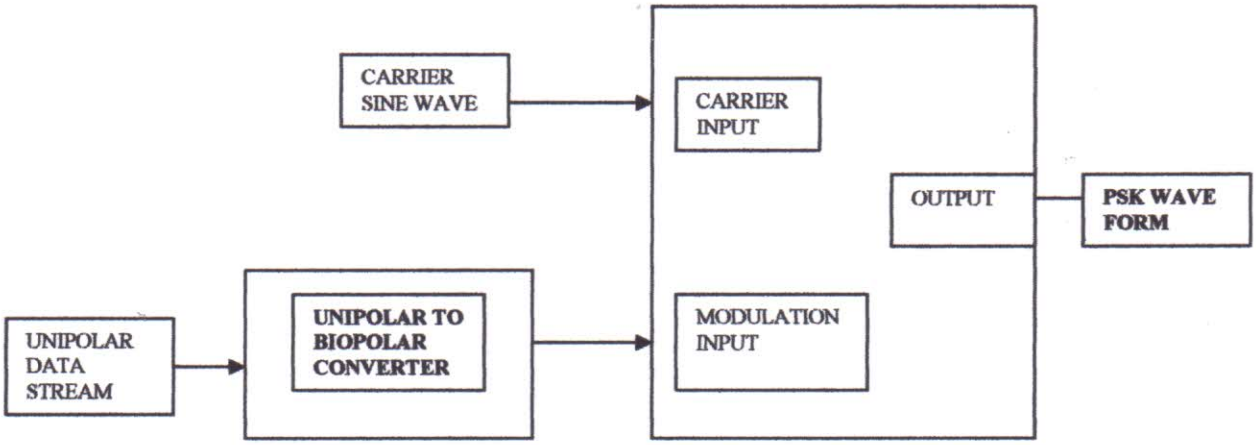
4.	Spectrum analyzer	3 GigaHZ, GWInstech

Theory: Phase shift Keying involve the phase change of the carrier sine wave between **0°** and **180°** in according with the data stream to be transmitted.

Functionally, the PSK modulator is very similar to the ASK modulator. Both uses balanced modulator to multiply the carrier with the modulating signal. But in contrast to ASK technique, the digital signal applied to the modulation input for PSK generation is bipolar i.e have equal positive and negative levels. When the modulating input is positive the output of modulator is a sine wave in phase with the carrier input. Where as for negative voltage levels, the output of the modulator is a sine wave which is shifted out of phase by 180° from the carrier input. This happen because the carrier input is now multiplied by the negative constant level. Thus the output in phase when a change in polarity of the modulating signal results.



PSK MODULATOR

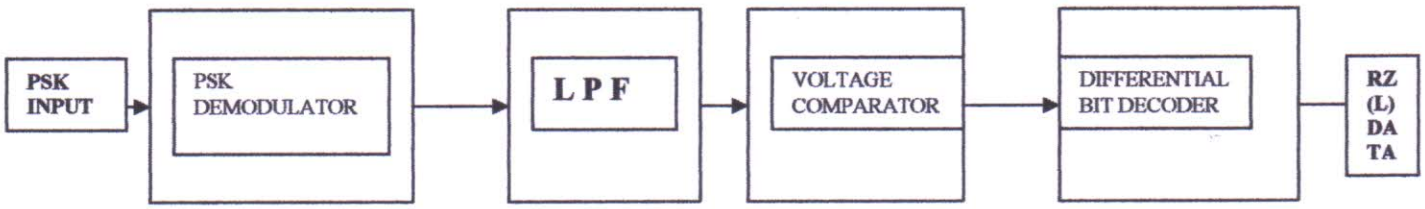
The Unipolar-Bipolar converts the unipolar data stream to bipolar data. At receiver, the square loop detector is used to demodulated the transmitted PSK signal.

The incoming PSK signal with 0° & 180° phase change is first fed to the signal square, which multiplies the input signal by itself. The ouput of this block is signal of twice the freq with the freq of the output doubled, the 0° & 180° phase change are reflect as 0° & 360° phase change. Since phase change of 360° is same as 0°, itcan be said the signal suarer simply removes the phase transition from the original PSK wave from.

The PLL block locks to the frequency of the signal square out put & produce a clean square wave output of same frequency as the incoming PSK signal, the PLL's output is divided by two in frequency domain is the divided by 2 circuit.

The PHASE ADJUST CIRCUIT allows the phase of the digital signal to be adjusted with respect to the input PSK signal. Also its output controls the closing of an analog switch. When the PHASE ADJUST block's output is low the switch opens and the detector's out put falls to 0 volts. The demodulator contains positive half cycle when the PSK input has one phase and only negative half cycle.when PSK input has another phase, the phase adjust pot meter is adjusted properly. The average level information of the demodulator output which contain the digital data information is extracted by the following low pass filter which is Squaredup by a voltage comparator.

As the sine wave is symmetrical it create a phase ambiguity which can be corrected by applying some data conditioning to the incoming stream to convert it to a from which recognizes the logic level by changes that occur & not by the absolute value. One such code is NRZ (M) where a change or the absence of change conveys the information. A change in level represent data '1' and no change represent data '0'. This NRZ (M) wavefrom is used to change the phase at the modulator. The comparator output at receiver can again be two forms, one being the logical inverse of the other. The receiver looks for changes in levels, a level change a '1' and no change '0', thus the phase ambiguity problem does not makes difference any more.



PSK RECEIVER SYSTEM

From the differential Bit Decoder output is a data '1' when it encounters a level change and a '0' when no change occurs. Thus the output from differential bit decoder is a NRZ(L) waveform.

Procedure: See at the last page

Observation :- i) Observe and plot the input Data and modulated signal wave form with a CRO.
ii) Observe and plot the demodulated Data at the Output.
iii)Observe the power spectral density of modulated signal with a spectrum analyzer.
v) Apply a sinosidal signal as input and measure the % of distortion of the demodulated signal.

I/P Signal Freq	I/P Signal Amplitude	Demodulated signal Amp	% of distortion

CONCLUSION :-

Questions :-

1. Draw block diagram of PSK receiver
2. Write the equation of the transmitted signal s(t) for PSK
3. What is Bits per symbol for PSK
4. What is the minimum BW requirement for PSK

PROCEDURE TO CARRY OUT EXPERIMENT ON TRAINER KIT ST 2103, 2104, 2106 & 2107 :-

(1) The experiment makes use of four trainers namely **ST2103, ST2104, ST2106 & ST2107.** **ST2103** TDM Pulse Code Modulation Transmitter Trainer serves as a data source while ST2104 TDM Pulse Code Modulation Receiver Trainer serves as analog signal recoverer. ST2106 serves as data formatting (Conditioning) device while ST2107 reformats (decondition) the data.

ST2103 & ST2106 Trainers serves as transmitter for our system & ST2107 & ST2104 Trainer serves as receiver.

(2) Ensure that all trainers are switched OFF, until the complete connection are made.

(3) Check ST2104 Trainer's CLOCK REGENERATION CIRCUIT Set up for correct operation as given in experimentation 1 of ST2103 / 4 work book

(4) Set up the following conditions on ST2103 trainer

(A) **MODE** switch set in **FAST** position.

(B) **PSEUDO - RANDOM SYNC CODE GENERATOR** switched **'ON'.**

(C) **ERROR CHECK CODE SELECTOR** switches **A & B in A=0 & B=0 Positions.**

(D) All switched faults 'OFF'

(5) Set ST2106 trainer's MODE switch in position ' 1 '

(6) Set up following conditions on ST2104 trainers :

(A) **MODE** switch set in **FAST** position

(B) **PSEUDO - RANDOM SYNC CODE DETECTOR IN 'ON'** position.

(C) **ERROR CHECK CODE SELECTOR** switch A & B IN A = 0 & B = 0 position.

(D) All switched faults kept 'OFF'

(7) Make the following connections between ST2103 A, ST2106 trainers.

ST2103 Trainer **ST2106 Trainer**

(A) TX CLOCK OUTPUT (t.p. 3) TO TX .CLOCK INPUT

(B) PCM OUTPUT (t.p. 44) TO TX .DATA INPUT

(8) Connect the TX TO OUTPUT (t.p 4) on ST2103 trainer to external trigger input of the oscilloscope. Set to negative edge triggered mode in oscilloscope. It may be necessary to adjust the trigger level manually to obtain a stable waveform.

(9) On ST2103 trainer make following connections :

(A) DC 1 to CH 0 INPUT

(B) CH 0 input to CH 1 input

This is done to supply the same voltage level to each of the two time division multiplexed channels. Thus we are able to get the same data stream for any time frame.

(10) Make the rest of the connections as shown in configuration Fig 3.

(11) Switch 'ON' the power

(12) On ST2103 trainer adjust the D.C.1 potentiometer until the 7 bit code displayed on A / D CONVERTER LED's is

D6	D5	D4	D3	D2	D1	DO
0	1	0	0	0	1	1

(13) Observe the DATA CLOCK output at t.p 4 on ST2106 trainer's DATA FORMAT block with oscilloscope. Adjust the oscilloscopes time base & position control until each rising edge of data clock coincides with one of scope's. vertical graticule line as shown in **Figure 4.** Each main division on scope's horizontal axis now represent one data bit time. Adjust the trigger level (manually, if necessary, to obtain a stable trace.) This sets convenient reference against which to observe the other wave forms.

1, Also set PULSE GENERATOR DELAY ADJUST fully Clockwise in step 6. In STEP 5 Set the switch in ST2107 trainer PSK Demodulator Block to 960KHz position.

(14) Switch off the power. **Make the additional connections as shown in Fig 36 as follows:**

(A) On ST2106 trainer :

(i) Carrier input of Modulator 1 (t.p.26) to 960KHz (I) carrier (t.p.17)

(ii) NRZ (M) output (t.p.6) to Unipolar-Bipolar Converter input (t.p.20)

(iii) Unipolar-Bipolar Converter output (t.p.21) to Modulator 1 input (t.p.27)

(B) Between ST2106 & ST2107 trainers :

(i.) Modulator 1 output (t.p.28) to PSK Demodulator input (t.p.10)

(C) On ST2107 trainer :

(i) PSK Demodulator output (t.p.15) to Low Pass Filter 1 input (t.p.23)

(ii) Low Pass Filter 1 output (t.p.24) to comparator 1 input (t.p.46)

(iii) Comparator 1 output (t.p.47) to Bit Decoder input (t.p.39)

(D) Between ST2107 and ST2104 trainers :

(i) Bit Decoder output (t.p.40) to PCM.DATA INPUT (t.p.1)

(ii) Bit Decoder input (t.p.39) to Clock Regeneration Circuit input (t.p.3)

(iii) Bit Decoder Clock input (t.p.41) to Clock Regeneration Circuit output (t.p.8)

Clock Regeneration Circuit output (t.p.8) to CLOCK input (t.p.46)

(15) Switch 'ON' the trainers.

(16) Monitor the Modulator 1 output (t.p.28) in ST2106 trainer with reference to its input (t.p.27) by using a dual trace oscilloscope. The three controls in modulator block may require some setting.

A) **GAIN :** This controls the amplitude of the modulator output signal very it until the amplitude of the output is 2 Vpp.

(B) **MODULATION OFF SET :** This controls the peak to peak amplitudes of 0° & 180° phases relative to each other. Vary it till the amplitudes for both faces become equal.

(C) **CARRIER OFF SET :** This controls the d.c. off sets of two phases namely 0° & 180° phases, relative to each other. Vary the control till the d.c. off set for them is reduced to as close as zero volts.

Displaying the NRZ (M) input with the PSK modulated waveform helps to understand the PSK modulation concept. Notice that every time the NRZ (M) waveform level changes, PSK modulated waveform undergoes a 180° phase change.

(17) To see the PSK Demodulation process, examine the input of PSK demodulator (t.p. 10) on ST2107 trainer with the demodulator's output (t.p. 15). Adjust the PHASE ADJUST control & see its effect on the demodulator's output.

Check the various test points provided at the output of the functional blocks of the PSK demodulator. This will help you fully grasp the PSK demodulation technique.

(18) The output of the demodulator goes to the Low Pass Filter 1's input. Monitor the filter's output (t.p.24) with reference to its input (t.p.28) Notice that the filter has extracted the average information from the demodulator output. Adjust the PSK demodulator's PHASE ADJUST control until the amplitude of filter's output is maximum.

(19) The low pass filter's output rounded & cannot be used for digital processing. In order to 'square up' the waveform COMPARATOR's are used (Data Squaring Circuit). The BIAS Control is adjusted so that the comparator's output pulse width at t.p.47 is same as the NRZ (M) pulse width.

(20) Switch 'ON' the PSEUDO-RANDOM SYNC CODE GENERATOR. Notice that the data on A/D CONVERTER LED's is same as that of the D/A CONVERTER LE.D.'s. You can verify this by varying the D.C.1 pot on ST2103 trainer. The data on ST2104 trainer always copy the ST2103 trainer's data output. This proves that the transmitter & receiver are now in frame synchronisation.

(21) Switch 'OFF' the trainers. Select internal triggering mode for the oscilloscope disconnect the CH.0 & CH.1 inputs on ST2103 trainer Instead connect CH.0 to ~1KHz signal & CH.1 to ~2KHz signal.

(22) Switch ON the power. Notice the outputs CH.0 & CH.1 on ST2104 trainers. They are replica of the input signals froms ST2103 trainers. Also notice that they are independent of each other (i.e. free from interference) & variation in one does not affect the other. If some interference is present, it can be removed ADJUST on ST2104 trainer.

(23) The same experiment can be done by using Biphase (Mark) code. Just remember to reformat the signal as described in Biphase (Mark) Chapter.

(24) The carrier frequency used in the above experiment was 960KHz. 1.44 MHz carrier can well be used. The only change to be made is to put the PSK demodulator switch in 1.44 MHz position.

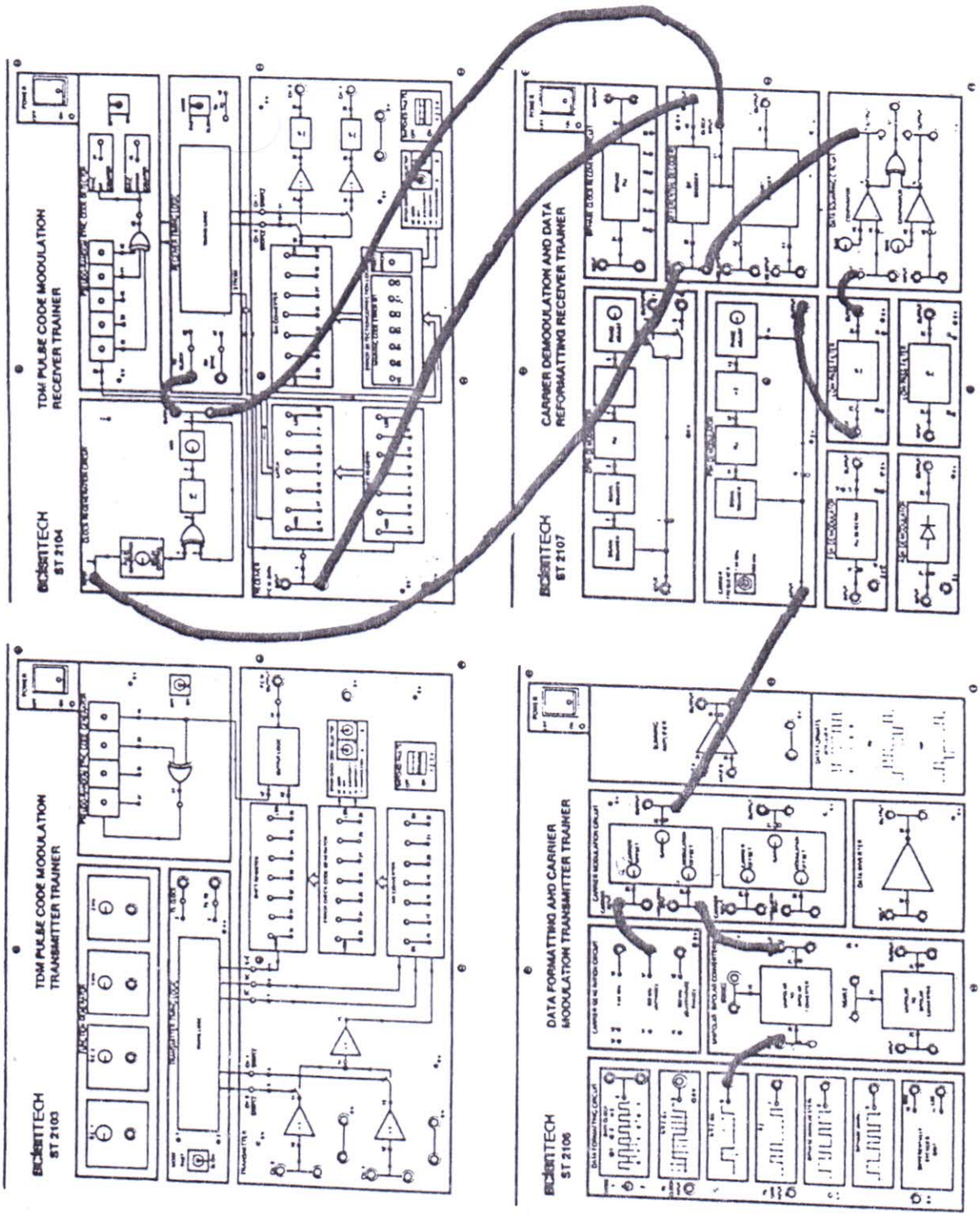

TDM PULSE CODE MODULATION
RECEIVER TRAINER
scientech
ST 2104
CARRIER DEMODULATION AND DATA
REFORMATTING RECEIVER TRAINER
scientech
ST 2107
TDM PULSE CODE MODULATION
TRANSMITTER TRAINER
scientech
ST 2103
DATA FORMATTING AND CARRIER
MODULATION TRANSMITTER TRAINER
scientech
ST 2106

Fig. 36

QUADRATURE PHASE SHIFT KEYING (QPSK)

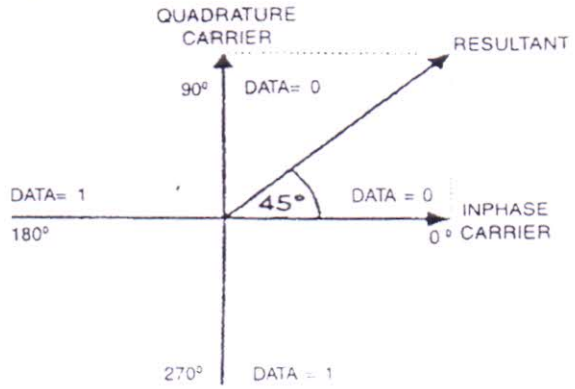
In quardrature Phase Shift keying each pair of consecutive data bit is treated as a two-bit (or dibit) code which is used to switch the phase of the carrier sinewave between one of four phases 90^0 apart. The four possible combination of dibit code are 00,01,10 and 11. Each code represents either a phase of 45^0, 135^0, 225^0, and 315^0 lagging, relative to the phase of the original unmodulated carrier. The choice of these phases is arbitrary as it is convenient to produce them. Quadrature Phase shift keying offers an advantage over PSK, in a manner that now each phase represents a two bit code rather than a single bit. This means now either we can change phase per second or the same amount of data can be transmitted with half as many phase changes per second. The second choice results in a lowering of bandwidth requirement.

The four phases are produced by adding two carrier waves of same frequency but 90^0 out of phases. The 0^0 phase carrier is called In-phase carrier and is labelled 1 The other is 90^0 (lagging) phase carrier termed as the Quadrature carrier and is labelled Q.

The carrier is controlled by the MSB (most significant bit) of the dibit code When the MSB is a level '0' the phase is 0 degrees when the MSB goes to level 1 the phase reverses to 180^0

The Q-carrier starts with 90^0 out of phase (with respect to reference I carrier). This carrier is controlled by the LSB (least significant bit) of the dibit code when the 1sb is a level 0, the phase is 90^0 degrees with reference to I-carrier). When the 1sb goes to a level 1, the phase reverses to 270^0 See **Fig 37**

Assume the digit code be 0. This would give a 0° phase to the in phase carrier and 0° phase to quadrature carrier (90° out of phase with respect to I-carrier). If we add these two waves we would get a 45° resultant. See fig 38.



Phasor Diagram

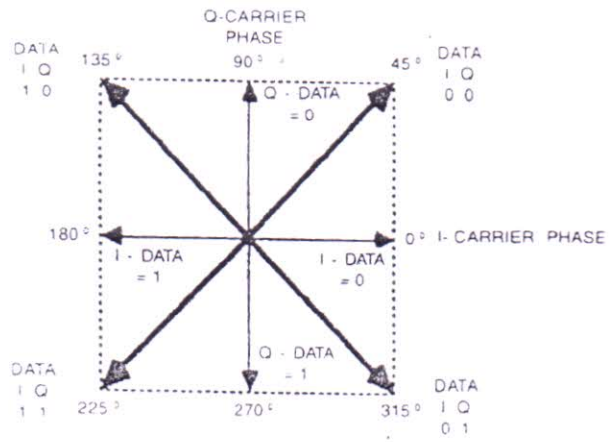
Fig 38

Similarly, the phase shifts for other three possible combinations would be as summed in the table below :

NRX (L)	Dibit Code	Phase
0	0	45°
0	1	315°
1	0	135°
1	1	225°

Table 2

At any instance of time, there is always a +/- 90° phase difference between the two modulation outputs. As a result, the amplitude of the resultant phasor will always be $\sqrt{2}$ times the amplitude of input phase or if they are equal. The creation of four phases by vector addition is as shown in fig 39

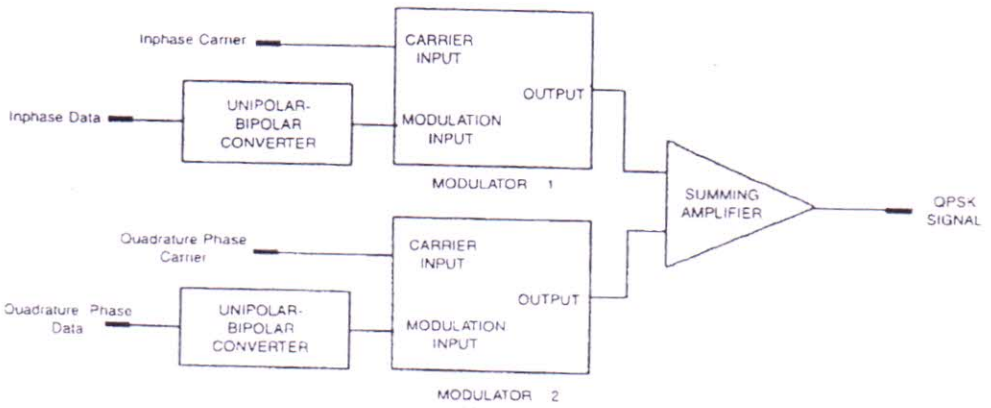


Phasor Diagram

Fig 39

It can be appreciated from the above phasor diagram that each phasor switches its phase depending on the data level exactly in the same way as the same way as the PSK modulator does. The only difference is that QPSK is sum of two such PSK modulators.

The QPSK modulator can be configured as shown in the fig 40



QPSK Modulator

Fig 40

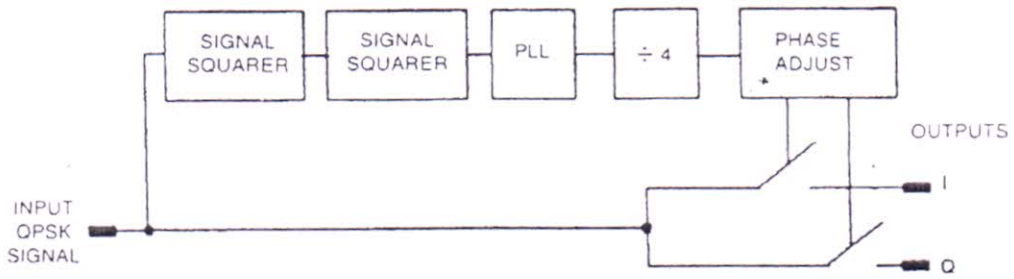
The two carriers namely I & Q as has been stated, have same frequency but differ in phase by 90°. Also the I data refer to the dibit MSB & Q data refers to the dibit LSB.

Each modulator performs phase-shift keying on its respective carrier input in accordance with respective data input such that,

a. The output of modulator 1 is a PSK signal with phase shift of 0° and 180° respectively, relative to the I-carrier, and

b. The output of modulator 2 is a PSK signal with phase shift of 90° and 270° respectively, relative to the I-carrier.

The output of the two modulators is summed by a summing amplifier. As it is clear from the earlier phasor diagram, the phase of the summing amplifier's output signal relative to I-carrier, at any instance of time takes one of the four phases 45° 135°, 225°, and 315° depending on the applied debit code. When these dibit codes alter, the phase of the QPSK output changes by 0°, 90°, 180° or 270° from its previous phase position. Thus the output of the summing amplifier is a QPSK waveform. The demodulation of QPSK signal is performed by the fourth power loop detector. The demodulator is quite similar to the one used in PSK system as can be seen from fig 41



QPSK Demodulator

Fig. 41

The incoming QPSK signal is first squared in the signal squarer 1. The functioning of the signal squarer has already been discussed in the PSK Modulator section. The output of the signal squarer 1 is a signal at twice the original frequency with phase changes reduced to 0° & 180°. This is because all the phase changes are also doubled. The 0° & 180° phase changes becomes 0° (as 2 x 180° = 360° = 0° phase shift.) and the 90° and 270° phases both become 180° (since 270° + 270° = 540° = 180° phase shift)

The output of the signal squarer 1 is fed to signal 1. The output of the signal squarer 1 is fed to signal squarer 2. This circuit is identical to signal squarer with frequency double that of the signal at its input (Quadrupled with respect to the original QPSK input signal frequency). The 0° and 180° phases changes are also reduced to a 0° phase changes are also reduced to 0° phases shift, since the phases are also doubled (Also 2 x 180° = 360° = 0° phase shift).

Therefore, the output from signal squarer 2 is a sinewave at four times the frequency of the original QPSK carrier signal with no phase changes.

The output of signal squarer 2 is fed to the phase locked loop (PLL) which locks on the incoming signal & produces a square wave of same frequency as that of the input.

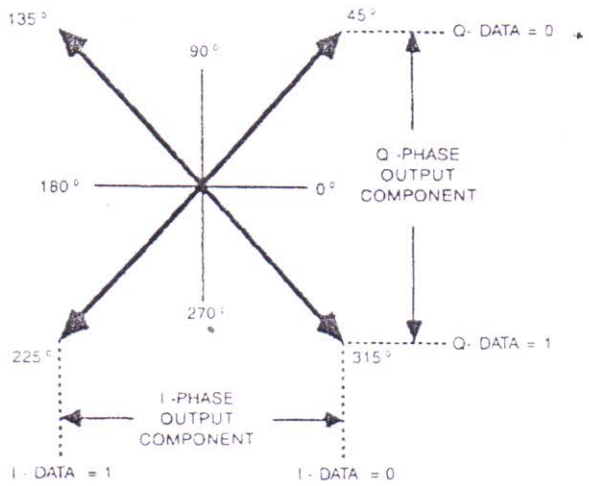
The output of PLL is divided in frequency by a factor of 4 by a ÷ 4 circuit. Now the frequency is same as that of the QPSK carrier signal.

The next stage in demodulation is a phase adjusts Circuit. The output of the phase adjust circuit are two square waves of same frequency as the input signal applied and

with 90° phase shift between them. Also the phase of the two output signals can also be adjusted relative to the original QPSK signal. Note that the 90° phase difference between the two outputs is maintained.

The output of the phase circuit controls the two analog switches. The switch is closed when the corresponding output goes high. The original QPSK signal is then switched through to one of the QPSK demodulator. How output can be input with a low level, the switches are open & the output is pulled down to 0V.

The two outputs from the demodulator are labeled I & Q. Once the correct phase relation between QPSK signal & phase adjust output have been set, the I & Q outputs will contain information about original two bit code. This is illustrated in phase or diagram. See fig 42.



All Angles represent phase LAG with respect to 0°

Phasor Diagram

Fig 42

The average level of the I & Q outputs contains information about the dibit code. The average level of the two outputs is extracted by passing them through the low pass filter. The output of the filters is rounded & cannot be used for digital processing. The wave 'Squared Up' by a voltage a comparator circuit.

A problem arises at this point. Since the phase information is lost in demodulator, the receiver does not know which phase is which as a result it might interpret any of the four phases e.g. 45° QPSK wave. Since there are four possible combinations our chances of recovering correct code is mere 25% e.g. if the receiver treats one of the three QPSK Phases to be at 45° phase, then the possibilities which arise are :

a. 'Q' data at 'I' data output 'I' data at 'Q' data output & inverted.

b. 'I' data at 'Q' data output 'Q' data at 'I' data output & inverted.

c. 'I' data at 'Q' data at correct outputs but both data streams inverted.

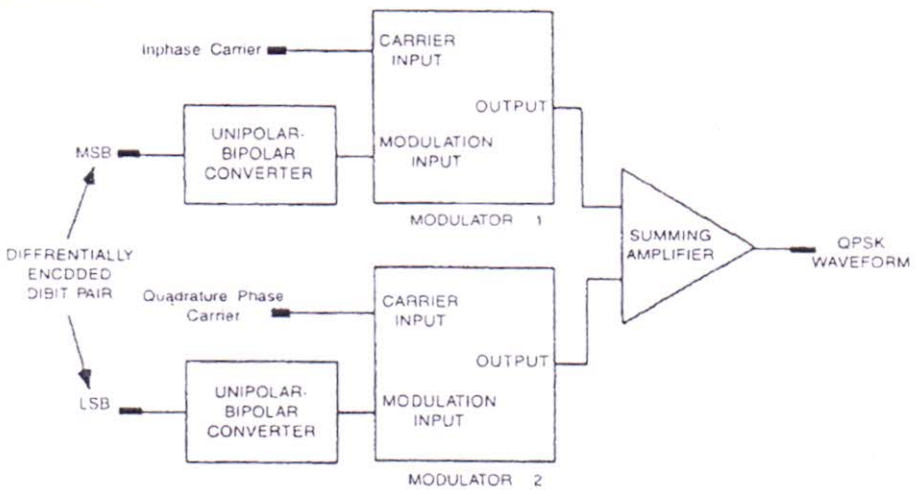
This leads to phase ambiguity. To overcome this problem, the NRZ (L) data is first encoded into differentially encoded dibit format at transmitter. In this format, each

dibit pair as encoded as a change in the code. This means that we make the phase change depend on the two bit code at the input instead of making the phase dependent on two bit code. i.e. still make use of dibit code but now they mean changes in phase rather than actual phase

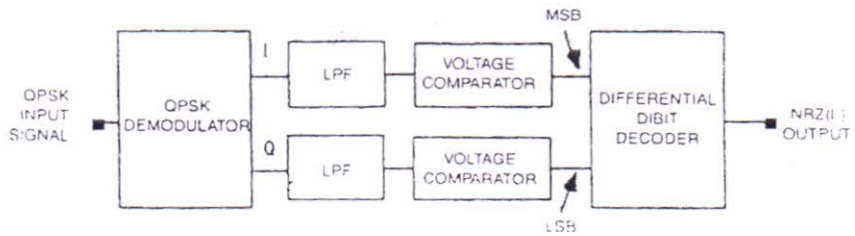
Code NRZ (L) Code		Old Meaning The Phase	New Meaning The Phase Change
0	0	45°	No Change
0	1	315°	90°
1	0	135°	180°
1	1	225°	270°

Table 3

At the receiver, once again there are four possibilities the two outputs may be interchanged or inverted as mentioned above. But now the absolute levels of the received data are no longer important. The receiver simply has to tell the two bit code change. As a result phase ambiguity is no longer a problem. To derive NRZ (L) waveform from the encoded pair a differential dibit decoder is used at receiver. Its output is serially transmitted. The fig 43 shows the functional block diagrams of the QPSK system.



QPSK TRANSMITTER



QPSK Receiver

Fig. 43

EXPERIMENT NO 10

Object:

To Study QPSK Modulation and Demodulation

Procedure :

Steps (1) to (13) : Follow the set up procedure for steps 1 to 13 as given in experiment 1, Also Set pulse generator delay adjust fully clock wise in step 6.

14. Make the additional connections as shown in fig. 44 as shown in following steps.

   a. On **ST2106** trainer :

      i) Differentially encoded dibit MSB (tp10) to unipolar bipolar converter 1 input (tp20)

      ii) Unipolar-Bipolar converter 1 output (tp21) to modulator 1 input (tp27).

      iii) Differentially encoded dibit LSB (tp11) to unipolar -bipolar 2 input (tp23).

      iv) Unipolar-Bipolar converter 2 output (tp24 to modulator 2 input (tp30).

      v) . 960KHz (1) output (tp17) to modulator 1 carrier input (tp26).

      vi) 960KHz (Q) output (tp18) to modulator 2 carrier input (tp29)

      vii) Modulator 1 output (tp28) to summing amplifier's input A (tp34).

      viii) Modulator 2 output (tp31) to summing amplifier's input B (tp35).

   b. Between **ST2106** & **ST2107:**

      i) Summing amplifier's output (tp36) to QPSK demodulator input (tp1).

   c. On **ST2107** trainer :

      i) QPSK demodulator output 1 (tp8) to low pass filter 1 input (tp23).

      ii) QPSK demodulator's Q output (tp9) to low pass filter 2 input (tp23).

      iii) Low pass filter 1 output (tp24) to comparator 1 input (tp46).

      iv) Low pass filter 2 output (tp28) to comparator 2 input (tp49).

      v) Data squaring circuit comparator 1 output (tp47) to differential decoder MSB input (tp42).

      vi) Data squaring circuit comparator 2 output (tp50) to differential decoder LSB input (tp43).

   d. Between **ST2107** & **ST2104** Trainers :

      i) Comparator 1 output (tp47) to clock regeneration circuit input (tp3).

      ii) Dibit decoder output (tp47) to PCM data input (tp3)

iii) Dibit decoder clock input (tp41) to clock regeneration circuit output (tp8).

e. On **ST2104** trainer :

i) Clock regeneration circuit output (tp8) to RX clock input (tp46).

15. Monitor the output of modulator 1 (tp28) in **ST2106** trainer. Adjust the scope's trigger level manually to obtain a stable display Use the controls provided in the modulator as shown in followings steps.

a. Gain: This controls the overall amplitude of the modulated waveform. Adjust it till you obtain a 2VPP signal.

b. Modulation off set : This controls the peak to peak amplitude of the 0° & 180° phases, relative to each other. Adjust this pot such that the amplitudes of the two phases are equal.

16. Make the same adjustments for modulator 2's output (tp31) by monitoring its outputs on the oscilloscope.

17. Monitor the output of the summing amplifier (tp36). The output is a QPSK Signal with 0°, 90°, 180° & 270° phase shifts clearly visible.

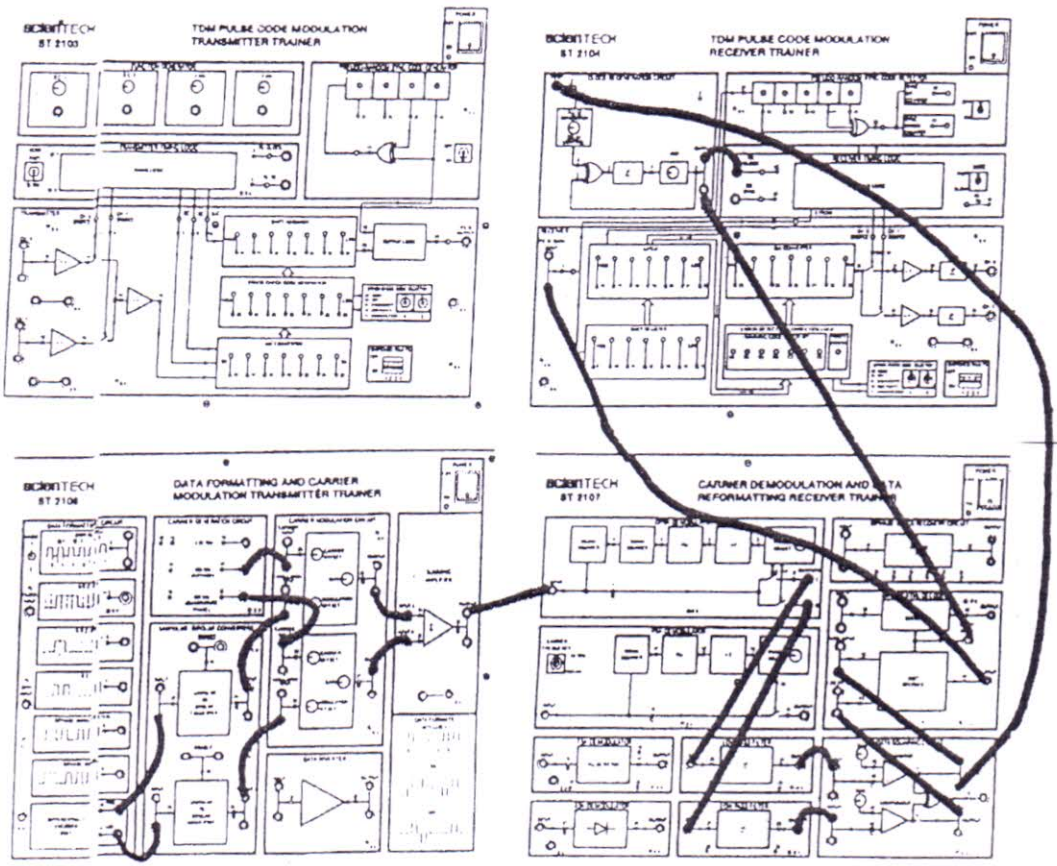


Fig. 44

18. To observe the QPSK demodulation process, monitor each output (tp8 & 9) of the QPSK demodulator with reference to input signal (tp1) on **ST2107**. Also monitor the test points provided at various block outputs, to understand the process of demodulation clearly.

19. Observe the two low pass filter's outputs (tp24 & 28). Adjust the phase adjust control provided on QPSK demodulator block until you obtain two levels only at low pass filter's outputs. The incorrect placement of phase adjust control produces multilevel output at filter output.

20. Monitor both the comparator's output (tp47 & 50). Adjust the bias level control of both comparators till their output doesn't have the correct pulse width.

    Now that the filter's output is balanced around 0 Volts. Adjustment of bias level to produce 0 V terminal of the comparator help achieving 'Squared up' version of the filter's output signal. This can be compared by simultaneously displaying the filter's output & the comparator's output on the oscilloscope.

21. Temporarily disconnect & then reconnect the QPSK input to the QPSK demodulator. Observe that after some trial you will obtain four different combinations at comparator's outputs (tp47 & 50). This explains the phase ambiguity in QPSK system.

22. To resolve the phase ambiguity problem the outputs from the comparators (tp47 & 50) are fed to the two inputs (tp42 & 43) of the differential dibit decoder which is driven by the regenerated clock from the **ST2104** trainer. It is synchronized to the rising edge of the signal at output of **ST2107** trainers comparator 1.

    On observing the differential dibit decoder's output (tp44) along with the NRZ(L) waveform (tp5) on the other channel you will notice that the output is nothing but the delayed NRZ (L) waveform.

    Try disconnecting & reconnecting the QPSK modulation output for a short period. Notice that this time the decoders output is unchanged. This is become the Differential decoder looks for the change in tap bit code rather than the absolute value. Thus the phase ambiguity problem is solved.

23. Turn ON the **ST2103** pseudo-random sync code generator. The transmitter & receiver one locked in 'frame synchronization'. This can be checked by verifying that A/D converter LED's on **ST2104** & trainer now carry the same data. Try varying the DC input to the **ST2103** trainer. The **ST2104** trainer should follow the changes.

24. Turn OFF the trainers. Discount the CH.0 & CH.1 inputs of **ST2103** trainer. Connect CH.0 input to ~2KHz signal.

25. Turn ON the trainers. Observe the CH.0 & CH.1 outputs (tp33 & 36) at **ST2104** trainers. The output should be identical to the input signal fed to each channel. The notice that the two signals are independent of each other & verification of one do not affect the other. If some interference is present it can be removed by varying the phase generator delay adjust control on **ST2104** trainer.

LAB MANUAL

for

Computer Network

Department of ECE

Siliguri Institute of Technology

S.No	Experiment
1	Study of different types of Network cables and Practically implement the cross-wired cable and straight through cable using clamping tool.
2	Study of Network Devices in Detail.
3	Study of network IP.
4	Connect the computers in Local Area Network.
5	Study of basic network command and Network configuration commands.
6	Configure a Network topology using packet tracer software.
7	Configure a Network topology using packet tracer software.
8	Configure a Network using Distance Vector Routing protocol.
9	Configure Network using Link State Vector Routing protocol.

Hardware and Software Requirement

Hardware Requirement

RJ-45 connector,
Climping Tool,
Twisted pair Cable

Software Requirement

Command Prompt And Packet Tracer.

EXPERIMENT-1

Aim: Study of different types of Network cables and Practically implement the cross-wired cable and straight through cable using clamping tool.

Apparatus (Components): RJ-45 connector, Climping Tool, Twisted pair Cable
Procedure: To do these practical following steps should be done:

1. Start by stripping off about 2 inches of the plastic jacket off the end of the cable. Be very careful at this point, as to not nick or cut into the wires, which are inside. Doing so could alter the characteristics of your cable, or even worse render is useless. Check the wires, **one more time** for nicks or cuts. If there are any, just whack the whole end off, and start over.

2. Spread the wires apart, but be sure to hold onto the base of the jacket with your other hand. You do not want the wires to become untwisted down inside the jacket. Category 5 cable must only have 1/2 of an inch of 'untwisted' wire at the end; otherwise it will be 'out of spec'. At this point, you obviously have ALOT more than 1/2 of an inch of un-twisted wire.

3. You have 2 end jacks, which must be installed on your cable. If you are using a pre-made cable, with one of the ends whacked off, you only have one end to install - the crossed over end. Below are two diagrams, which show how you need to arrange the cables for each type of cable end. Decide at this point which end you are making and examine the associated picture below.

Diagram shows you how to prepare Cross wired connection

RJ45 Pin # (END 1)	Wire Color	Diagram End #1	RJ45 Pin # (END 2)	Wire Color	Diagram End #2
1	White/Orange		1	White/Green	
2	Orange		2	Green	
3	White/Green		3	White/Orange	
4	Blue		4	White/Brown	
5	White/Blue		5	Brown	
6	Green		6	Orange	
7	White/Brown		7	Blue	
8	Brown		8	White/Blue	

Diagram shows you how to prepare straight through wired connection

RJ45 Pin # (END 1)	Wire Color	Diagram End #1	RJ45 Pin # (END 2)	Wire Color	Diagram End #2
1	White/Orange		1	White/Green	
2	Orange		2	Green	
3	White/Green		3	White/Orange	
4	Blue		4	White/Brown	
5	White/Blue		5	Brown	
6	Green		6	Orange	
7	White/Brown		7	Blue	
8	Brown		8	White/Blue	

EXPERIMENT-2

Aim: Study of following Network Devices in Detail

- Repeater
- Hub
- Switch
- Bridge
- Router
- Gate Way

Apparatus (Software): No software or hardware needed.

Procedure: Following should be done to understand this practical.

1. **Repeater:**Functioning at Physical Layer.A **repeater** is an electronic device that receives a signal and retransmits it at a higher level and/or higher power, or onto the other side of an obstruction, so that the signal can cover longer distances. Repeater have two ports ,so cannot be use to connect for more than two devices

2. Hub: An **Ethernet hub**, **active hub**, **network hub**, **repeater hub**, **hub** or **concentrator** is a device for connecting multiple twisted pair or fiber optic Ethernet devices together and making them act as a single network segment. Hubs work at the physical layer (layer 1) of the OSI model. The device is a form of multiport repeater. Repeater hubs also participate in collision detection, forwarding a jam signal to all ports if it detects a collision.

3. **Switch:**A **network switch** or **switching hub** is a computer networking device that connects network segments.The term commonly refers to a network bridge that processes and routes data at the data link layer (layer 2) of the OSI model. Switches that additionally process data at the network layer (layer 3 and above) are often referred to as Layer 3 switches or multilayer switches.

4. **Bridge:** A **network bridge** connects multiple network segments at the data link layer (Layer 2) of the OSI model. In Ethernet networks, the term *bridge* formally means a device that behaves according to the IEEE 802.1D standard. A bridge and switch are very much alike; a switch being a bridge with numerous ports. *Switch* or *Layer 2 switch* is often used interchangeably with *bridge*.Bridges can analyze incoming data packets to determine if the bridge is able to send the given packet to another segment of the network.

5. **Router:** A **router** is an electronic device that interconnects two or more computer networks, and selectively interchanges packets of data between them. Each data packet contains address information that a router can use to determine if the source and destination are on the same network, or if the data packet must be transferred from one network to another. Where multiple routers are used in a large collection of interconnected networks, the routers exchange information about target system addresses, so that each router can build up a table showing the preferred paths between any two systems on the interconnected networks.

6. **Gate Way:** In a communications network, a network node equipped for interfacing with

another network that uses different protocols.

- A gateway may contain devices such as protocol translators, impedance matching devices, rate converters, fault isolators, or signal translators as necessary to provide system interoperability. It also requires the establishment of mutually acceptable administrative procedures between both networks.
- A protocol translation/mapping gateway interconnects networks with different network protocol technologies by performing the required protocol conversions.

EXPERIMENT- 3

Aim: Study of network IP

- Classification of IP address
- Sub netting
- Super netting

Apparatus (Software): NA

Procedure: Following is required to be study under this practical.

- Classification of IP address

As show in figure we teach how the ip addresses are classified and when they are used.

Class	Address Range	Supports
Class A	1.0.0.1 to 126.255.255.254	Supports 16 million hosts on each of 127 networks.
Class B	128.1.0.1 to 191.255.255.254	Supports 65,000 hosts on each of 16,000 networks.
Class C	192.0.1.1 to 223.255.254.254	Supports 254 hosts on each of 2 million networks.
Class D	224.0.0.0 to 239.255.255.255	Reserved for multicast groups.
Class E	240.0.0.0 to 254.255.255.254	Reserved.

- Sub netting

Why we Develop sub netting and How to calculate subnet mask and how to identify subnet address.

- Super netting

Why we develop super netting and How to calculate supernet mask and how to identify supernet address.

EXPERIMENT-4

Aim: Connect the computers in Local Area Network.

Procedure: On the host computer

On the host computer, follow these steps to share the Internet connection:

1. Log on to the host computer as Administrator or as Owner.
2. Click **Start**, and then click **Control Panel**.
3. Click **Network and Internet Connections**.
4. Click **Network Connections**.
5. Right-click the connection that you use to connect to the Internet. For example, if you connect to the Internet by using a modem, right-click the connection that you want under Dial-up / other network available.
6. Click **Properties**.
7. Click the **Advanced** tab.

8. Under **Internet Connection Sharing**, select the **Allow other network users to connect through this computer's Internet connection** check box.

9. If you are sharing a dial-up Internet connection, select the **Establish a dial-up connection whenever a computer on my network attempts to access the Internet** check box if you want to permit your computer to automatically connect to the Internet.

10. Click **OK**. You receive the following message:

When Internet Connection Sharing is enabled, your LAN adapter will be set to use IP address 192.168.0.1. Your computer may lose connectivity with other computers on your network. If these other computers have static IP addresses, it is a good idea to set them to obtain their IP addresses automatically. Are you sure you want to enable Internet Connection Sharing?

11. Click **Yes**.
The connection to the Internet is shared to other computers on the local area network (LAN).

The network adapter that is connected to the LAN is configured with a static IP address of 192.168.0.1 and a subnet mask of 255.255.255.0

On the client computer

To connect to the Internet by using the shared connection, you must confirm the LAN adapter IP configuration, and then configure the client computer. To confirm the LAN adapter IP configuration, follow these steps:

1. Log on to the client computer as Administrator or as Owner.
2. Click **Start**, and then click **Control Panel**.

3. Click **Network and Internet Connections**.
4. Click **Network Connections**.
5. Right-click **Local Area Connection** and then click **Properties**.
6. Click the **General** tab, click **Internet Protocol (TCP/IP)** in the **connection uses the following items** list, and then click **Properties**.

7. In the **Internet Protocol (TCP/IP) Properties** dialog box, click **Obtain an IP address automatically** (if it is not already selected), and then click **OK**.

Note: You can also assign a unique static IP address in the range of 192.168.0.2 to 192.168.0.254. For example, you can assign the following static IP address, subnet mask, and default gateway:

8. IP Address 192.168.31.202
9. Subnet mask 255.255.255.0
10. Default gateway 192.168.31.1

11. In the **Local Area Connection Properties** dialog box, click **OK**.

12. Quit Control Panel.

EXPERIMENT- 5

Aim: Study of basic network command and Network configuration commands.

Apparatus (Software): Command Prompt And Packet Tracer.

Procedure: To do this EXPERIMENT- follows these steps:

In this EXPERIMENT- students have to understand basic networking commands e.g ping, tracert etc.

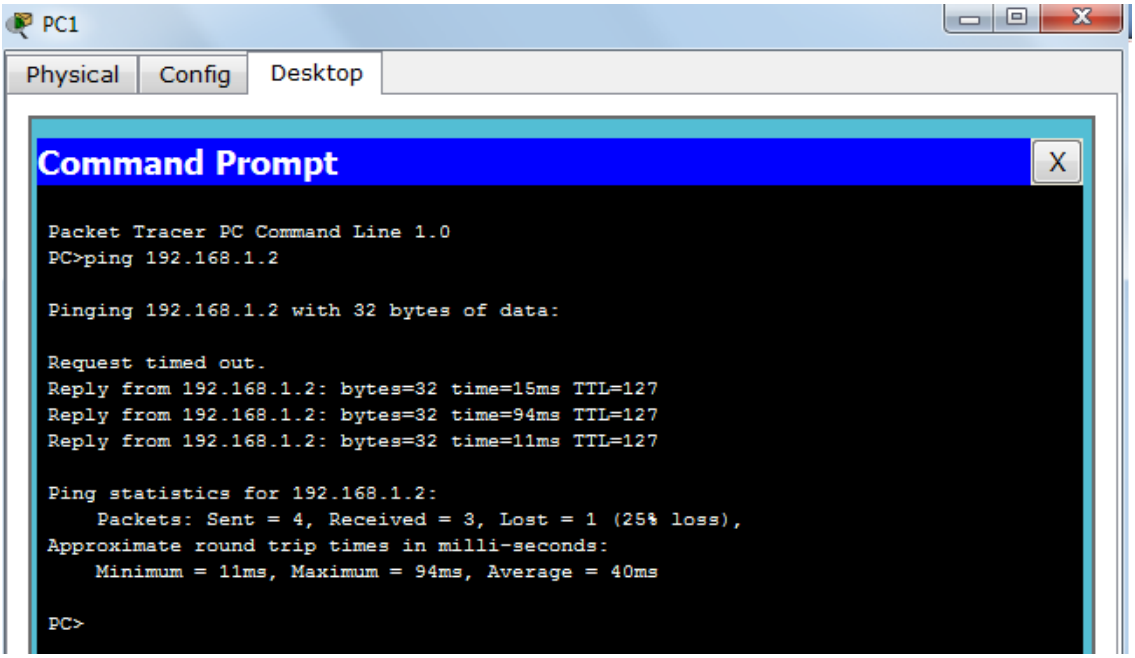
All commands related to Network configuration which includes how to switch to privilege mode and normal mode and how to configure router interface and how to save this configuration to flash memory or permanent memory.

This commands includes

- Configuring the Router commands
- General Commands to configure network
- Privileged Mode commands of a router
- Router Processes & Statistics
- IP Commands
- Other IP Commands e.g. show ip route etc.

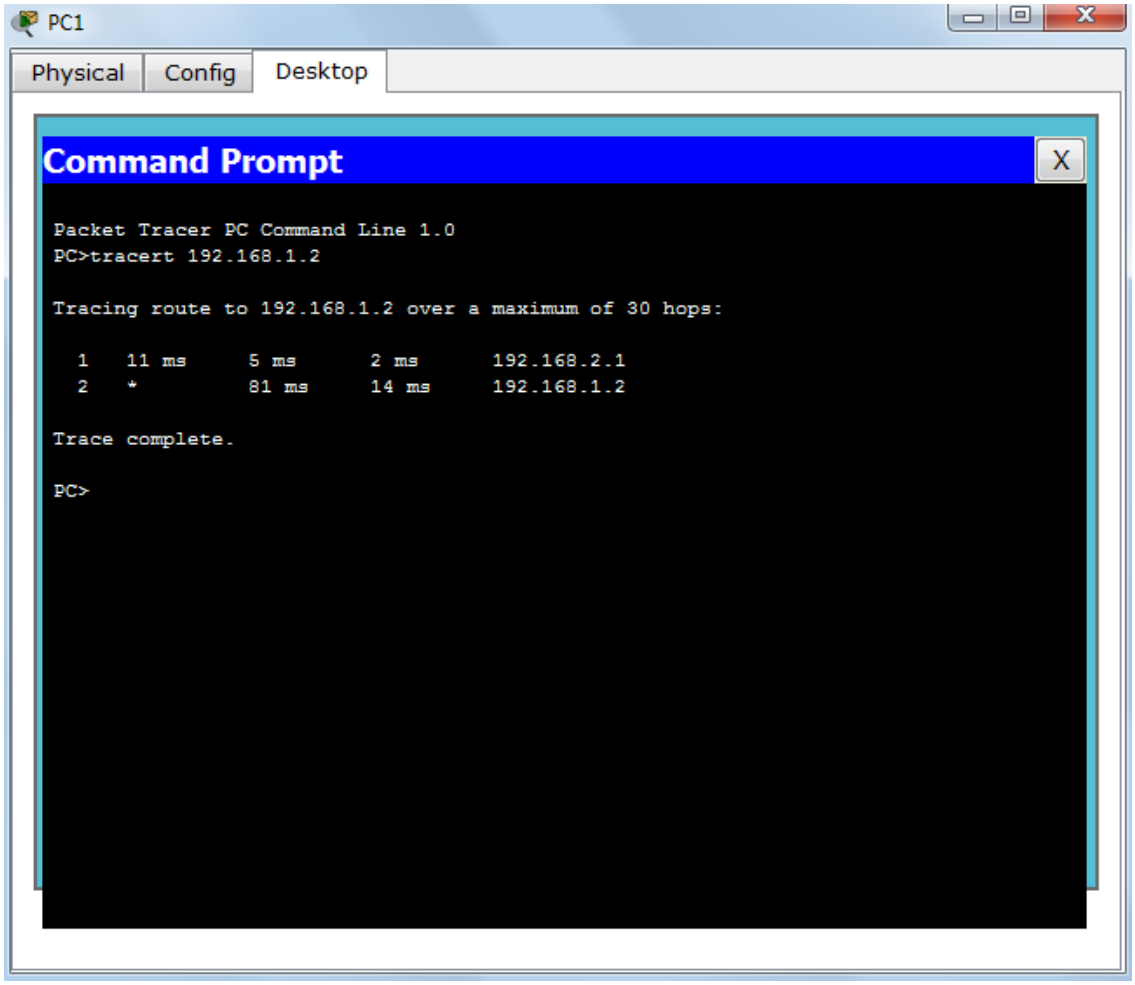
ping:

ping(8) sends an ICMP ECHO_REQUEST packet to the specified host. If the host responds, you get an ICMP packet back. Sound strange? Well, you can “ping” an IP address to see if a machine is alive. If there is no response, you know something is wrong.



Traceroute:

Tracert is a command which can show you the path a packet of information takes from your computer to one you specify. It will list all the routers it passes through until it reaches its destination, or fails to and is discarded. In addition to this, it will tell you how long each 'hop' from router to router takes.

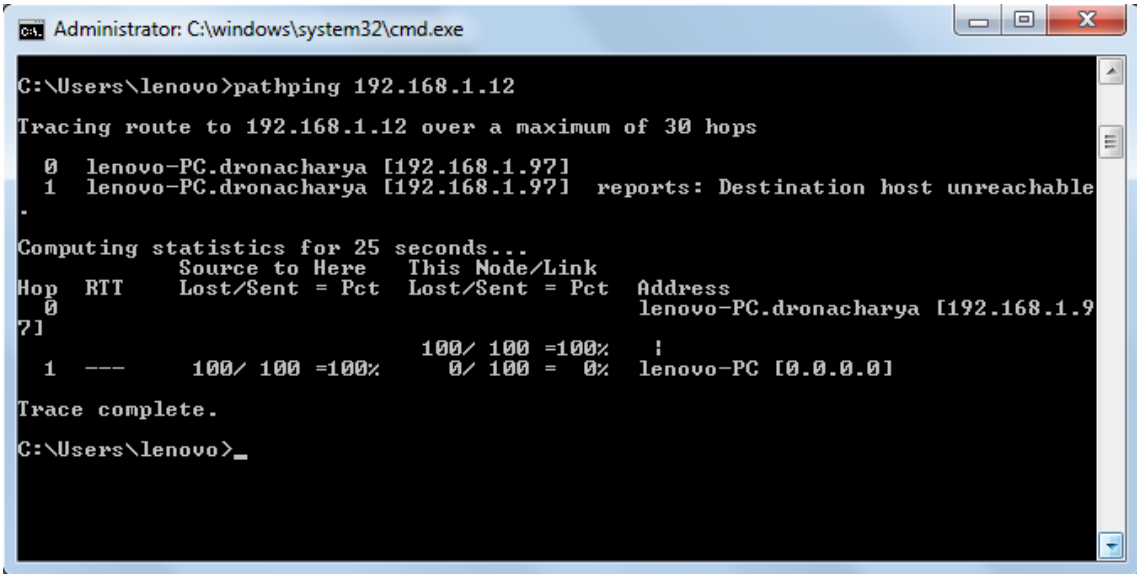


nslookup:

Displays information from Domain Name System (DNS) name servers.
NOTE :If you write the command as above it shows as default your pc's server name firstly.

pathping:

A better version of tracert that gives you statics about packet lost and latency.



Getting Help

In any command mode, you can get a list of available commands by entering a question mark (?).

Router>**?**

To obtain a list of commands that begin with a particular character sequence, type in those haracters followed immediately by the question mark (?).

Router#**co?**

configure connect copy
To list keywords or arguments, enter a question mark in place of a keyword or argument. Include a space before the question mark.

Router#**configure ?**

memory Configure from NV memory
network Configure from a TFTP network host
terminal Configure from the terminal
You can also abbreviate commands and keywords by entering just enough characters to make the command unique from other commands. For example, you can abbreviate the **show** command to **sh**.

Configuration Files

Any time you make changes to the router configuration, you must save the changes to memory because if you do not they will be lost if there is a system reload or power outage. There are two types of configuration files: the running (current operating) configuration and the startup configuration.
Use the following privileged mode commands to work with configuration files.

- **configure terminal** – modify the running configuration manually from the terminal.
- **show running-config** – display the running configuration.
- **show startup-config** – display the startup configuration.
- **copy running-config startup-config** – copy the running configuration to the startup configuration.
- **copy startup-config running-config** – copy the startup configuration to the running configuration.
- **erase startup-config** – erase the startup-configuration in NVRAM.
- **copy tftp running-config** – load a configuration file stored on a Trivial File Transfer Protocol (TFTP) server into the running configuration.
- **copy running-config tftp** – store the running configuration on a TFTP server.

IP Address Configuration

Take the following steps to configure the IP address of an interface.
Step 1: Enter privileged EXEC mode:

Router>**enable** password

Step 2: Enter the **configure terminal** command to enter global configuration mode.

Router#**config terminal**

Step 3: Enter the **interface** type slot/port (for Cisco 7000 series) or **interface** type port (for Cisco 2500 series) to enter the interface configuration mode.

Example:
Router (config)#**interface ethernet 0/1**
Step 4: Enter the IP address and subnet mask of the interface using the **ip address** ipaddress subnetmask command.

Example,
Router (config-if)#**ip address 192.168.10.1 255.255.255.0**

Step 5: Exit the configuration mode by pressing Ctrl-Z
Router(config-if)#**[Ctrl-Z]**

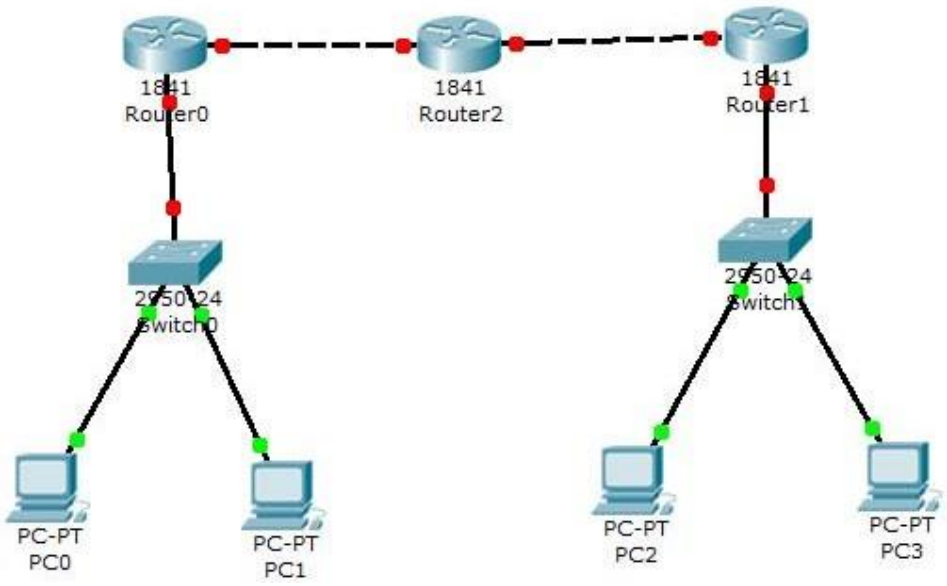
EXPERIMENT-6

Aim: Configure a Network topology using packet tracer software.

Apparatus (Software): Packet tracer Software

Procedure: To implement this practical following network topology is required to be configured using the commands learned in previous practical.

After configuring the given network a packet should be ping from any one machine to another.



Router0 Configuration Command :.....

Continue with configuration dialog? [yes/no]: no

```
Press RETURN to get started!

Router>

Router>Enable

Router#config t

Enter configuration commands, one per line. End with CNTL/Z.

Router(config)#hostname router0

router0(config)#interface fastethernet 0/0

router0(config-if)#ip address 192.168.1.1 255.255.255.0

router0(config-if)#description router0 fastethernet 0/0

router0(config-if)#no shutdown

%LINK-5-CHANGED: Interface FastEthernet0/0, changed state to up

router0(config-if)#exit

router0(config)#interface fastethernet 0/1

router0(config-if)#description router0 fastethernet 0/1

router0(config-if)#no shutdown

%LINK-5-CHANGED: Interface FastEthernet0/1, changed state to up

router0(config-if)#exit

router0(config)#exit

%SYS-5-CONFIG_I: Configured from console by console

router0#show running-config

Building configuration...

Current configuration : 437 bytes
```

```
!
version 12.4
no service password-encryption
!
hostname router0
!
!
!
!
!
ip ssh version 1
!
!
interface FastEthernet0/0
 description router0 fastethernet 0/0
 ip address 192.168.1.1 255.255.255.0
 duplex auto
 speed auto
!
interface FastEthernet0/1
 description router0 fastethernet 0/1
 no ip address
 duplex auto
 speed auto
!
interface Vlan1
 no ip address
```

```
 shutdown
!
ip classless
!
!
!
!
!
line con 0
line vty 0 4
 login
!
!
end



router0#
router0#
router0#copy running-config startup-config
Destination filename [startup-config]?
Building configuration...
[OK]
router0#
```

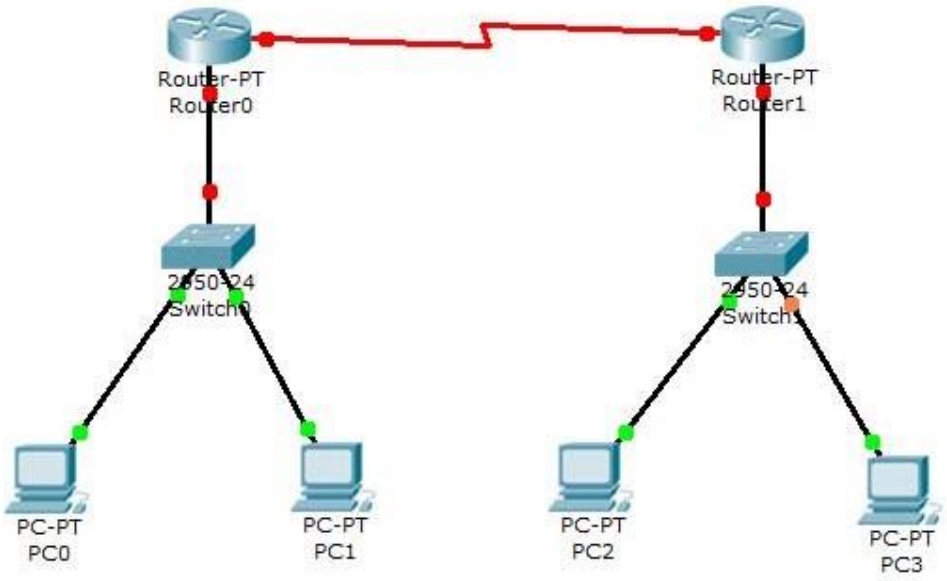
EXPERIMENT-7

Aim: Configure a Network topology using packet tracer software.

Apparatus (Software): Packet tracer Software

Procedure: To implement this practical following network topology is required to be configured using the commands learned in previous practical.

After configuring the given network a packet should be ping from any one machine to another.



Router0 Configuration Command.....

Router>enable
Router#configure terminal
Enter configuration commands, one per line. End with CNTL/Z.
Router(config)#interface FastEthernet0/0
Router(config-if)#ip address 192.168.0.254 255.255.255.0

Router(config-if)#no shutdown

%LINK-5-CHANGED: Interface FastEthernet0/0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/0, changed state to up
Router(config-if)#exit

```
Router(config)#exit
%SYS-5-CONFIG_I: Configured from console by console
Router#
Router#configure terminal
Enter configuration commands, one per line. End with CNTL/Z.
Router(config)#interface FastEthernet0/0
Router(config-if)#
Router(config-if)#exit
Router(config)#interface Serial2/0
Router(config-if)#ip address 192.168.1.1 255.255.255.0
Router(config-if)#no shutdown

%LINK-5-CHANGED: Interface Serial2/0, changed state to down
Router(config-if)#exit
Router(config)#exit
%SYS-5-CONFIG_I: Configured from console by console
Router#wr
Building configuration...
[OK]
Router#show running-config
Building configuration...

Current configuration : 542 bytes
!
version 12.2
no service password-encryption
!
hostname Router
!
!
!
!
!
ip ssh version 1
!
!
interface FastEthernet0/0
 ip address 192.168.0.254 255.255.255.0
 duplex auto
 speed auto
!
interface FastEthernet1/0
 no ip address
 duplex auto
 speed auto
 shutdown
!
interface Serial2/0
 ip address 192.168.1.1 255.255.255.0
!
```

```
interface Serial3/0
 no ip address
 shutdown
!
interface FastEthernet4/0
 no ip address
 shutdown
!
interface FastEthernet5/0
 no ip address
 shutdown
!
ip classless
!
!
!
!
!
line con 0
line vty 0 4
 login
!
!
end
```

Router#

Router1 Configuration Command.....

Continue with configuration dialog? [yes/no]: no

Press RETURN to get started!

```
Router>enable
Router#
Router#configure terminal
Enter configuration commands, one per line. End with CNTL/Z.
Router(config)#interface Serial2/0
Router(config-if)#ip address 192.168.1.2 255.255.255.0
Router(config-if)#no shutdown

%LINK-5-CHANGED: Interface Serial2/0, changed state to up
Router(config-if)#exit
Router(config)#exit
%SYS-5-CONFIG_I: Configured from console by console
Router#config t
```

```
Enter configuration commands, one per line. End with CNTL/Z.
Router(config)#
Router(config)#interface Serial2/0
Router(config-if)#
Router(config-if)#exit
Router(config)#interface FastEthernet0/0
Router(config-if)#ip address 192.168.2.254 255.255.255.0
Router(config-if)#no shutdown

%LINK-5-CHANGED: Interface FastEthernet0/0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/0, changed state to
up
Router(config-if)#exit
Router(config)#exit
%SYS-5-CONFIG_I: Configured from console by console
Router#wr
Building configuration...
[OK]
Router#
Router#show running-config
Building configuration...

Current configuration : 542 bytes
!
version 12.2
no service password-encryption
!
hostname Router
!
!
!
!
!
ip ssh version 1
!
!
interface FastEthernet0/0
 ip address 192.168.2.254 255.255.255.0
 duplex auto
 speed auto
!
interface FastEthernet1/0
 no ip address
 duplex auto
 speed auto
 shutdown
!
interface Serial2/0
 ip address 192.168.1.2 255.255.255.0
!
```

```
interface Serial3/0
 no ip address
 shutdown
!
interface FastEthernet4/0
 no ip address
 shutdown
!
interface FastEthernet5/0
 no ip address
 shutdown
!
ip classless
!
!
!
!
!
line con 0
line vty 0 4
 login
!
!
end


Router#
```

IP ROUTE Command.....

```
Router#config t
Enter configuration commands, one per line. End with CNTL/Z.
Router(config)#ip route 192.168.2.0 255.255.255.0 192.168.2.2
Router(config)#exit
Router#show ip route
Codes: C - connected, S - static, I - IGRP, R - RIP, M - mobile, B - BGP
       D - EIGRP, EX - EIGRP external, O - OSPF, IA - OSPF inter area
       N1 - OSPF NSSA external type 1, N2 - OSPF NSSA external type 2
       E1 - OSPF external type 1, E2 - OSPF external type 2, E - EGP
       i - IS-IS, L1 - IS-IS level-1, L2 - IS-IS level-2, ia - IS-IS inter area
       * - candidate default, U - per-user static route, o - ODR
       P - periodic downloaded static route

Gateway of last resort is not set

C    192.168.2.0/24 is directly connected, FastEthernet0/0
C    192.168.1.2/24 is directly connected, Serial2/0
S    192.168.2.0/24 [1/0] via 192.168.1.2
Router#
```

IP ROUTE Command.....

```
Router>enable
Router#show ip route
Codes: C - connected, S - static, I - IGRP, R - RIP, M - mobile, B - BGP
       D - EIGRP, EX - EIGRP external, O - OSPF, IA - OSPF inter area
       N1 - OSPF NSSA external type 1, N2 - OSPF NSSA external type 2
       E1 - OSPF external type 1, E2 - OSPF external type 2, E - EGP
       i - IS-IS, L1 - IS-IS level-1, L2 - IS-IS level-2, ia - IS-IS inter area
       * - candidate default, U - per-user static route, o - ODR
       P - periodic downloaded static route

Gateway of last resort is not set

S    192.168.0.0/24 [1/0] via 192.168.1.1
C    192.168.0.0/24 is directly connected, FastEthernet0/0
C    192.168.1.1/24 is directly connected, Serial2/0
Router#
```

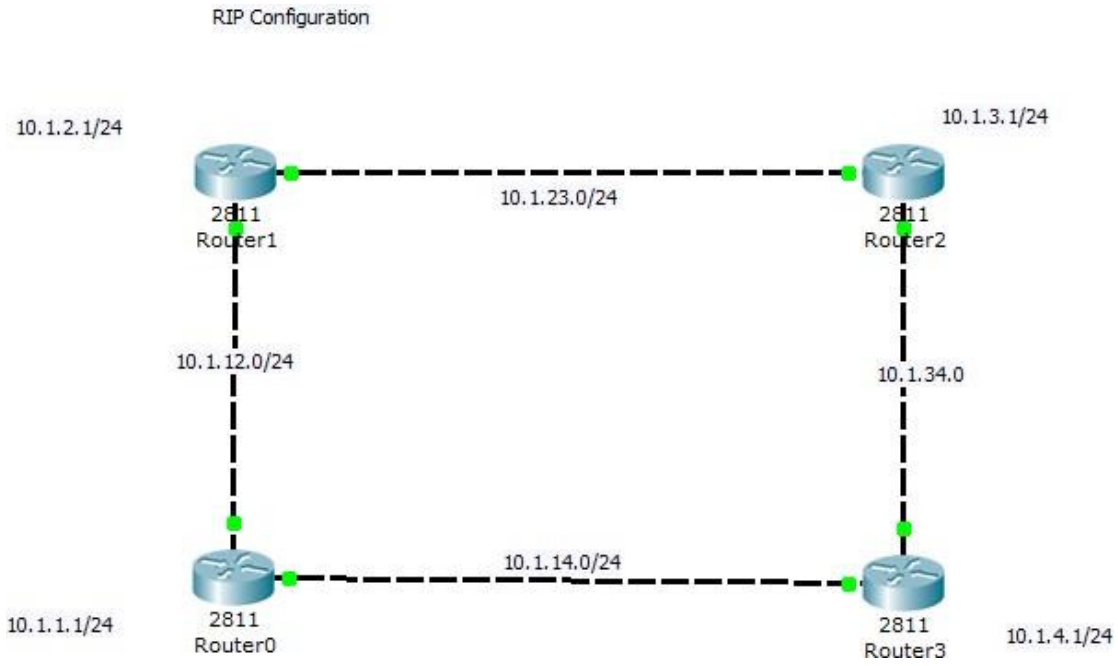
EXPERIMENT- 8

Aim: Configure a Network using Distance Vector Routing protocol.

- RIP

Apparatus (Software): packet tracer software

Procedure:
1. Develop a Topology shown in figure given below.
3. Configure all Routers
4. Implement RIP protocols in Router to configure Network.



Router0 configuration.....

Continue with configuration dialog? [yes/no]: no

Press RETURN to get started!

Router>
Router>en
Router#config t
Enter configuration commands, one per line. End with CNTL/Z.

```
Router(config)#hostname router0

router0(config)#int lo0

%LINK-5-CHANGED: Interface Loopback0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface Loopback0, changed state to up
router0(config-if)#ip address 10.1.1.1 255.255.255.0
router0(config-if)#int  f0/0
router0(config-if)#ip address 10.1.12.1 255.255.255.0
router0(config-if)#no shut

%LINK-5-CHANGED: Interface FastEthernet0/0, changed state to up
router0(config-if)#int f0/1
router0(config-if)#ip address 10.1.14.1 255.255.255.0
router0(config-if)#no shut

%LINK-5-CHANGED: Interface FastEthernet0/1, changed state to up
router0(config-if)#end
%SYS-5-CONFIG_I: Configured from console by console
router0#wr
Building configuration...
[OK]
router0#
router0#
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/1, changed state to up

router0 con0 is now available

Press RETURN to get started.

router0>
router0>en
router0#config t
Enter configuration commands, one per line.  End with CNTL/Z.
router0(config)#router rip
router0(config-router)#net 10.0.0.0
router0(config-router)#
router0(config-router)#end
%SYS-5-CONFIG_I: Configured from console by console
router0#show ip route
Codes: C - connected, S - static, I - IGRP, R - RIP, M - mobile, B - BGP
       D - EIGRP, EX - EIGRP external, O - OSPF, IA - OSPF inter area
       N1 - OSPF NSSA external type 1, N2 - OSPF NSSA external type 2
       E1 - OSPF external type 1, E2 - OSPF external type 2, E - EGP
       i - IS-IS, L1 - IS-IS level-1, L2 - IS-IS level-2, ia - IS-IS inter area
       * - candidate default, U - per-user static route, o - ODR
       P - periodic downloaded static route

Gateway of last resort is not set
```

```
    10.0.0.0/24 is subnetted, 3 subnets
C 10.1.1.0 is directly connected, Loopback0
C  10.1.12.0 is directly connected, FastEthernet0/0
C  10.1.14.0 is directly connected, FastEthernet0/1
router0#
router0#
```

Router1 Configuration.....

```
Continue with configuration dialog? [yes/no]: no


Press RETURN to get started!

Router>enable
Router#config t
Enter configuration commands, one per line.  End with CNTL/Z.
Router(config)#int lo0

%LINK-5-CHANGED: Interface Loopback0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface Loopback0, changed state to up
Router(config-if)#ip address 10.1.2.1 255.255.255.0
Router(config-if)#no shut
Router(config-if)#int  f0/1
Router(config-if)#ip address 10.1.23.1 255.255.255.0
Router(config-if)#no shut

%LINK-5-CHANGED: Interface FastEthernet0/1, changed state to up
Router(config-if)#int f0/0
Router(config-if)#ip address 10.1.12.2 255.255.255.0
Router(config-if)#no shut

%LINK-5-CHANGED: Interface FastEthernet0/0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/0, changed state to up
Router(config-if)#end
%SYS-5-CONFIG_I: Configured from console by console
Router#wr
Building configuration...
[OK]
Router#
Router#
Router#
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/1, changed state to up

Router con0 is now available

Press RETURN to get started.

Router>
Router>en
Router#con t
```

% Ambiguous command: "con t"
Router#co t
% Ambiguous command: "co t"
Router#conf t
Enter configuration commands, one per line. End with CNTL/Z.
Router(config)#router rip
Router(config-router)#net 10.0.0.0
Router(config-router)#
Router(config-router)#
Router(config-router)#end
%SYS-5-CONFIG_I: Configured from console by console
Router#

Router2 Configuration.....

Continue with configuration dialog? [yes/no]: no

Press RETURN to get started!

Router>en
Router#config t
Enter configuration commands, one per line. End with CNTL/Z.
Router(config)#int lo0

%LINK-5-CHANGED: Interface Loopback0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface Loopback0, changed state to up
Router(config-if)#ip address 10.1.3.1 255.255.255.0
Router(config-if)#no shut
Router(config-if)#int f0/0
Router(config-if)#ip address 10.1.23.2 255.255.255.0
Router(config-if)#no shut

%LINK-5-CHANGED: Interface FastEthernet0/0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/0, changed state to up
Router(config-if)#int f0/1
Router(config-if)#ip address 10.1.34.1 255.255.255.0
Router(config-if)#no shut

%LINK-5-CHANGED: Interface FastEthernet0/1, changed state to up
Router(config-if)#End
%SYS-5-CONFIG_I: Configured from console by console

Router#wr
Building configuration...
[OK]
Router#
Router#
Router#
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/1, changed state to up

```
Router con0 is now available


Press RETURN to get started.


Router>
Router>
Router>en
Router#show ip route
Codes: C - connected, S - static, I - IGRP, R - RIP, M - mobile, B - BGP
       D - EIGRP, EX - EIGRP external, O - OSPF, IA - OSPF inter area
       N1 - OSPF NSSA external type 1, N2 - OSPF NSSA external type 2
       E1 - OSPF external type 1, E2 - OSPF external type 2, E - EGP
       i - IS-IS, L1 - IS-IS level-1, L2 - IS-IS level-2, ia - IS-IS inter area
       * - candidate default, U - per-user static route, o - ODR
       P - periodic downloaded static route

Gateway of last resort is not set

     10.0.0.0/24 is subnetted, 3 subnets
C 10.1.3.0 is directly connected, Loopback0
C  10.1.23.0 is directly connected, FastEthernet0/0
C  10.1.34.0 is directly connected, FastEthernet0/1
Router#config t
Enter configuration commands, one per line.  End with CNTL/Z.
Router(config)#router rip
Router(config-router)#net 10.0.0.0
Router(config-router)#end
%SYS-5-CONFIG_I: Configured from console by console
Router#
Router#
Router#show ip route
Codes: C - connected, S - static, I - IGRP, R - RIP, M - mobile, B - BGP
       D - EIGRP, EX - EIGRP external, O - OSPF, IA - OSPF inter area
       N1 - OSPF NSSA external type 1, N2 - OSPF NSSA external type 2
       E1 - OSPF external type 1, E2 - OSPF external type 2, E - EGP
       i - IS-IS, L1 - IS-IS level-1, L2 - IS-IS level-2, ia - IS-IS inter area
       * - candidate default, U - per-user static route, o - ODR
       P - periodic downloaded static route

Gateway of last resort is not set

     10.0.0.0/24 is subnetted, 7 subnets
R       10.1.1.0 [120/2] via 10.1.23.1, 00:00:19, FastEthernet0/0
R       10.1.2.0 [120/1] via 10.1.23.1, 00:00:19, FastEthernet0/0
C       10.1.3.0 is directly connected, Loopback0
R       10.1.12.0 [120/1] via 10.1.23.1, 00:00:19, FastEthernet0/0
R       10.1.14.0 [120/2] via 10.1.23.1, 00:00:19, FastEthernet0/0
C       10.1.23.0 is directly connected, FastEthernet0/0
```

```
C       10.1.34.0 is directly connected, FastEthernet0/1
Router#
Router#
Router#
```

Router3 Configuration.....

```
Continue with configuration dialog? [yes/no]: no


Press RETURN to get started!

Router>
Router>en
Router#config t
Enter configuration commands, one per line.  End with CNTL/Z.
Router(config)#int lo0

%LINK-5-CHANGED: Interface Loopback0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface Loopback0, changed state to up
Router(config-if)#int f0/0
Router(config-if)#ip address 10.1.34.2 255.255.255.0
Router(config-if)#no shut

%LINK-5-CHANGED: Interface FastEthernet0/0, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/0, changed state to up
Router(config-if)#
Router(config-if)#int  f0/1
Router(config-if)#ip address 10.1.14.2 255.255.255.0
Router(config-if)#no shut

%LINK-5-CHANGED: Interface FastEthernet0/1, changed state to up
%LINEPROTO-5-UPDOWN: Line protocol on Interface FastEthernet0/1, changed state to up
Router(config-if)#end
%SYS-5-CONFIG_I: Configured from console by console
Router#wr
Building configuration...
[OK]
Router#
Router#
Router#show ip route
Codes: C - connected, S - static, I - IGRP, R - RIP, M - mobile, B - BGP
       D - EIGRP, EX - EIGRP external, O - OSPF, IA - OSPF inter area
       N1 - OSPF NSSA external type 1, N2 - OSPF NSSA external type 2
       E1 - OSPF external type 1, E2 - OSPF external type 2, E - EGP
       i - IS-IS, L1 - IS-IS level-1, L2 - IS-IS level-2, ia - IS-IS inter area
       * - candidate default, U - per-user static route, o - ODR
       P - periodic downloaded static route

Gateway of last resort is not set
```

```
    10.0.0.0/24 is subnetted, 2 subnets
C  10.1.14.0 is directly connected, FastEthernet0/1
C  10.1.34.0 is directly connected, FastEthernet0/0
Router#conf t
Enter configuration commands, one per line.  End with CNTL/Z.
Router(config)#router rip
Router(config-router)#net 10.0.0.0
Router(config-router)#

Router(config-router)#end
%SYS-5-CONFIG_I: Configured from console by console
Router#show ip route
Codes: C - connected, S - static, I - IGRP, R - RIP, M - mobile, B - BGP
       D - EIGRP, EX - EIGRP external, O - OSPF, IA - OSPF inter area
       N1 - OSPF NSSA external type 1, N2 - OSPF NSSA external type 2
       E1 - OSPF external type 1, E2 - OSPF external type 2, E - EGP
       i - IS-IS, L1 - IS-IS level-1, L2 - IS-IS level-2, ia - IS-IS inter area
       * - candidate default, U - per-user static route, o - ODR
       P - periodic downloaded static route

Gateway of last resort is not set

    10.0.0.0/24 is subnetted, 7 subnets
R       10.1.1.0 [120/1] via 10.1.14.1, 00:00:09, FastEthernet0/1
R       10.1.2.0 [120/2] via 10.1.34.1, 00:00:14, FastEthernet0/0
             [120/2] via 10.1.14.1, 00:00:09, FastEthernet0/1
R       10.1.3.0 [120/1] via 10.1.34.1, 00:00:14, FastEthernet0/0
R       10.1.12.0 [120/1] via 10.1.14.1, 00:00:09, FastEthernet0/1
C       10.1.14.0 is directly connected, FastEthernet0/1
R       10.1.23.0 [120/1] via 10.1.34.1, 00:00:14, FastEthernet0/0
C       10.1.34.0 is directly connected, FastEthernet0/0
Router#
```

EXPERIMENT- 9

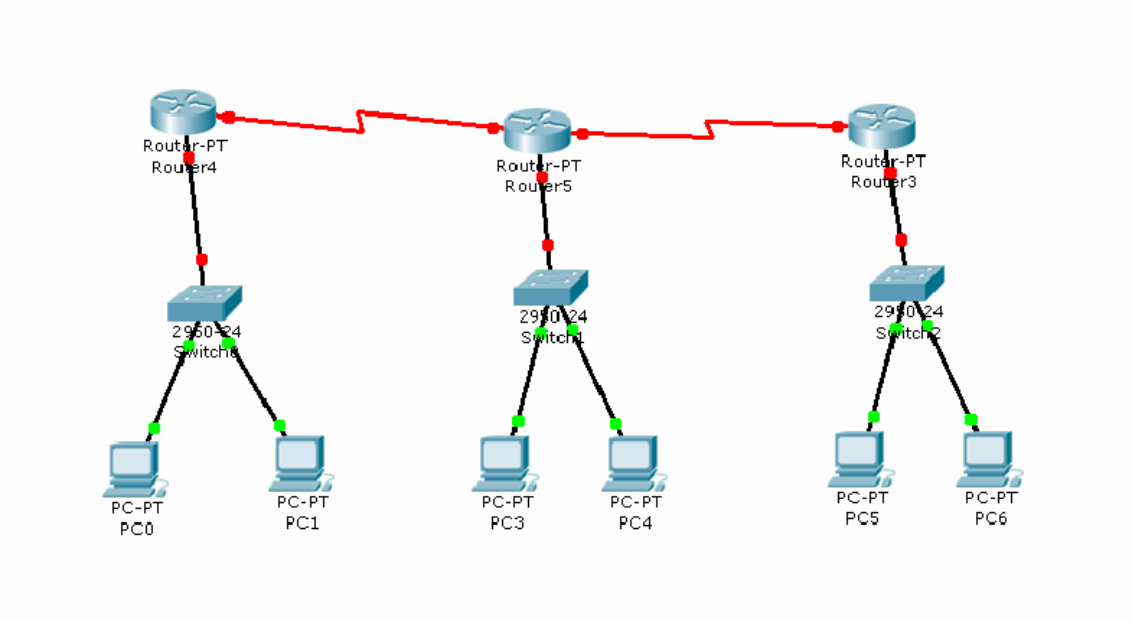
Aim: Configure Network using Link State Vector Routing protocol.

- OSPF

Apparatus (Software): Packet Tracer Software

Procedure:

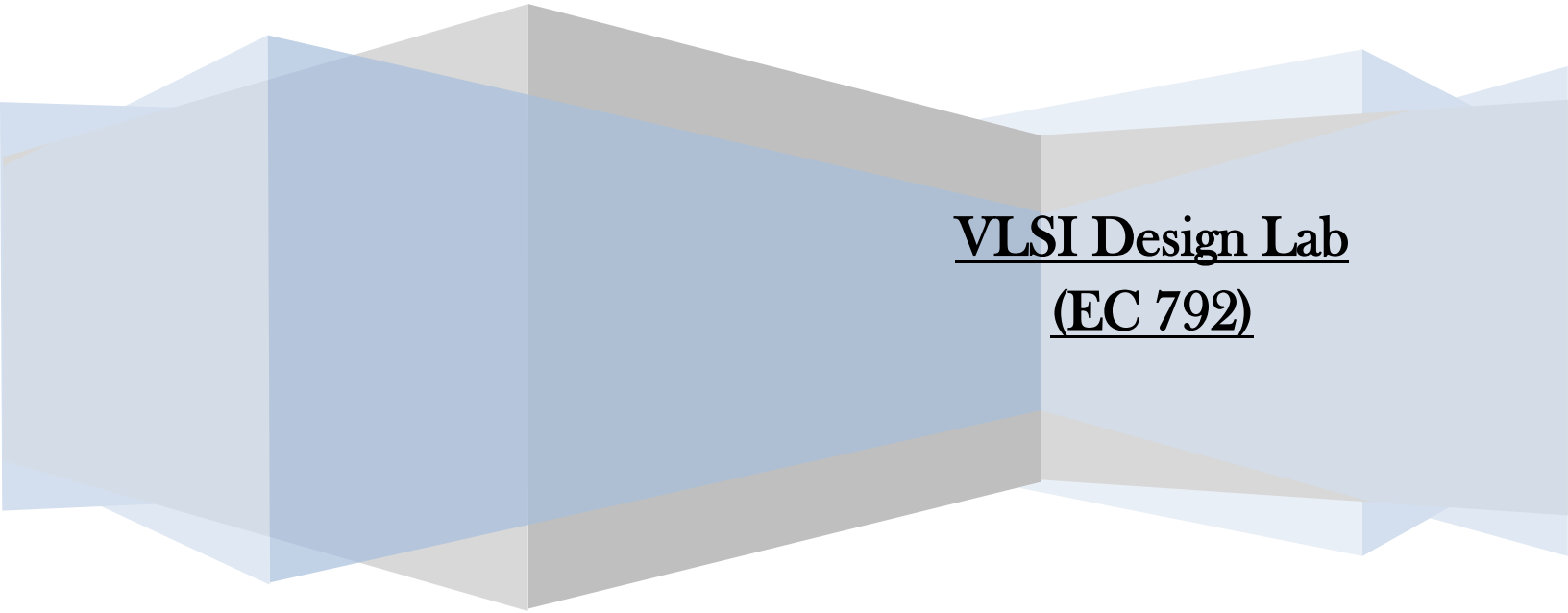
1. Develop a Topology shown in figure given below.
2. Configure all the workstations
3. Configure all switches
4. Configure all Routers
5. Implement OSPF protocols in Router to configure Network.



Laboratory Manual

PART - 1

FAMILIARITY WITH SPICE SIMULATION TOOL

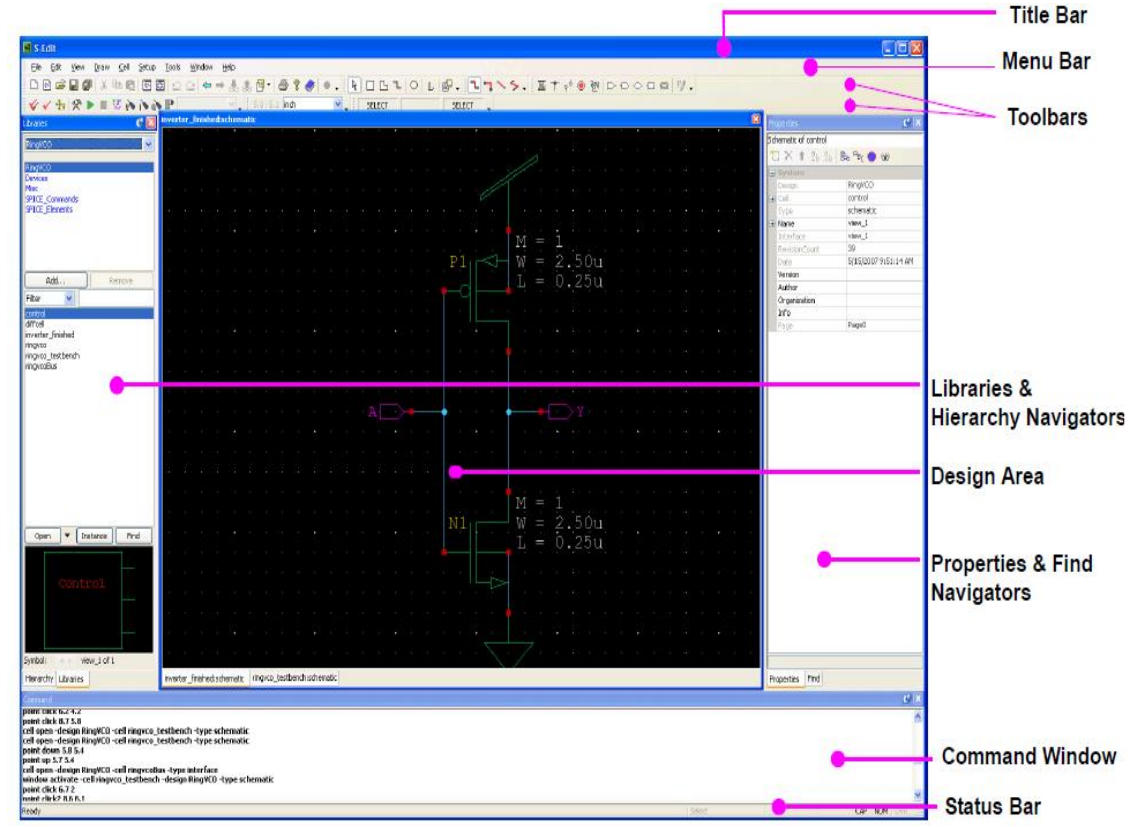


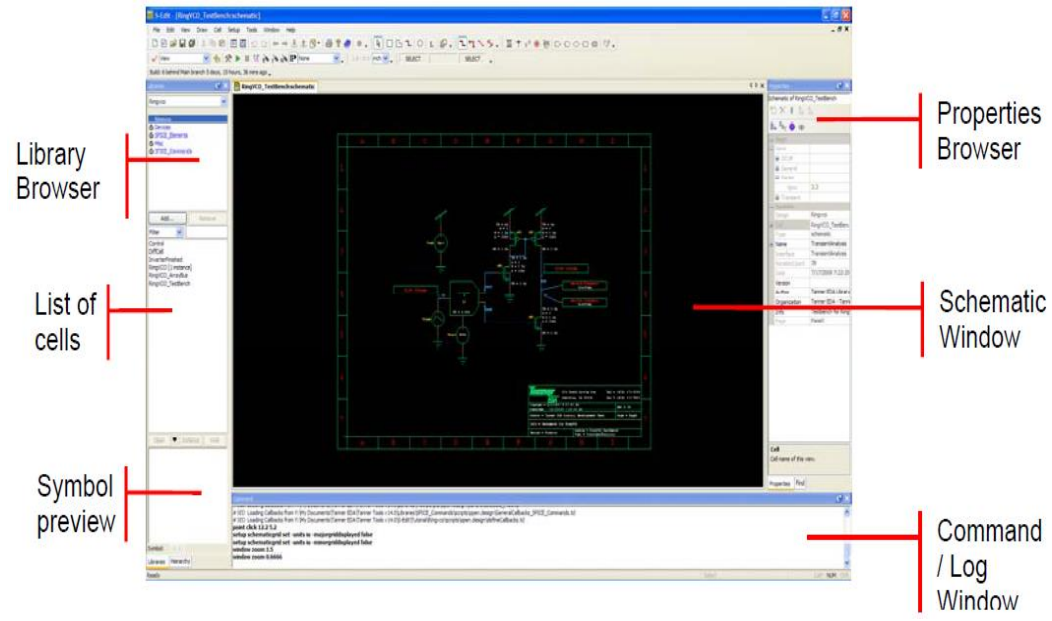
VLSI Design Lab
(EC 792)

VLSI Design Laboratory (EC-792)

Index

T-Spice User Guide
S-EDIT
Simulating Schematics in S-EDIT

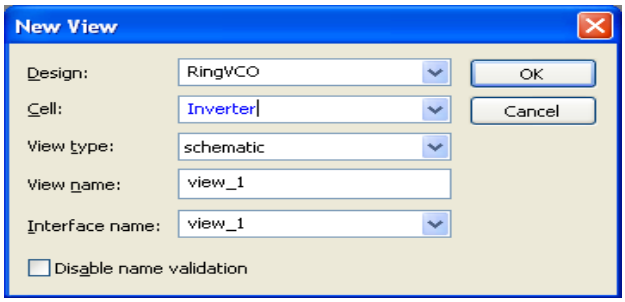




Creating a new Schematic Cell

1. Run Tanner Tools S-Edit, Tanner's schematic entry program. Invoke File -> new design
2. Type the design name and locate it in a specified folder and click OK.

3. Add libraries from libraries toolbar-Add (all.tanner), it includes complete library components. This all folder is located at: Specific Folder\Tanner EDA\Tanner Tools v14.1\Libraries\All
4. Now create a cell. Invoke **Cell > New View** : Give a name to cell0: (Inverter)



After pressing OK, you will get an empty drawing area for a new schematic view.

Placing Instances

5. Click on devices for CMOS Inverter design-Select PMOS and click on Instance.
6. **Instance Cell** dialog will appear, you can change the instance name or properties of the cell you are about to instance.
7. With mouse device will attached, place it by single click, right click on workspace or press "Esc" key or "done" button on the instance cell dialog to go back.
8. To move a component anywhere at workspace, click on component, then by pressing mouse scroll button or by pressing left mouse key, or select and press "Alt+M" key it can be moved anywhere.
9. Additional instances of PMOS can be placed by continuing to click the mouse to place instances.
10. When opening a view, you can force the new view to open in a new window by holding the **Ctrl** key down when opening the new view.
11. **Let's pan and zoom around the design.**
    - Use the +/- keys to zoom in and out of the design.
    - Scroll the mouse wheel to zoom in and out of the design, centered at the cursor.
    - Use the **arrow** keys to pan up/down/left/right.
    - Press and release the **Z** key, then click and drag the left mouse button over a region to zoom into that region ("create a zoom box").
    - Use the **Home** key to fit the entire contents to the window.
12. **Shortcut for Draw menu**
    - **Draw > Force Move ----------select and press Alt + M**
    - **Draw > Rotate ---------- select and press R**
    - **Draw > Flip > Flip Horizontal ------ select and press H**
    - **Draw > Flip > Flip Vertical ---------- select and press V**

    Edit > Undo (Ctrl + Z)
13. Similarly paste NMOS ->
14. Properties of devices can be changed from properties toolbar, it is customizable. But don't change the instance name or properties of the cell you are about to instance.
15. Select misc from library toolbar, and paste Vdd and Gnd
16. Select SPICE_Elements then voltage source, Type of voltage can be changed by instance cell, Paste one DC and one Pulse voltage source at workspace

Making Connections and placing Input, output ports

17. Now connections can be made from wire selection from Electrical Toolbar
18. Just click on open node of device and wire the nodes accordingly
19. Now add Input port and Output port

20. Now connect input, output port accordingly

Checking the Schematic

21. Invoke **Tools > Design Checks** and press the **Check view and hierarchy** button ( ), to perform a schematic check. The design checker will report warnings for the unconnected wire end, the unconnected symbol port, Instances with no name or non-unique name, Ports with the same name have the same type and the unconnected net label. You can jump to step 28 if you do not want to follow the steps to create symbol or step 31 to avoid writing Spice commands in netlist also.

Moving Instances with Rubberbanding

22. Select the PMOS and Vdd instances at the top of the schematic, as well as the attached wires, by drawing a selection box. First enter selection mode by pressing the **Select** toolbar button ( ), then press and hold down the left mouse button, drag a rectangle, then release the mouse button. Now press and hold the middle mouse button while dragging the mouse up or down to move the two instances without breaking any connections.

Creating a new Symbol

23. Invoke **Cell > New View**, and select the name (Eg. **Ringvco)** for design, **Inverter** for the cell, and symbol for view type. Enter **view_1** for View name and Interface name. After pressing OK, you will get an empty drawing area for a new symbol view

Automatic Symbol Generation and Update

24. Invoke **Cell > Update Symbol**, and S-Edit will create a symbol
25. Modify this symbol to make a symbol more suitable for an inverter. Draw a triangle for symbol using the path drawing tool. To draw a path, select the **Path** drawing button on the toolbar, (), then select the **All Angle** button on the segment toolbar, (), then click the left mouse button to place the first vertex, subsequent clicks with the left mouse button will place additional vertices. Clicking the right mouse button ends the wire without placing a vertex, and double clicking the left mouse button will end the path with placing a vertex at the double click location.
26. Delete the box that was placed by **Update Symbol**. Press the **Select** button on the toolbar (), click on the box to select it (it will highlight when selected) and press the delete key to delete the box. Move the ports and labels onto the new graphics you have drawn
27. Use **View Symbol** ( ) and **View Schematic** ( ) toolbar buttons to open the Symbol or Schematic view that corresponds to the currently active window. Pressing the **"?"** key will toggle between symbol and schematic views of a cell.

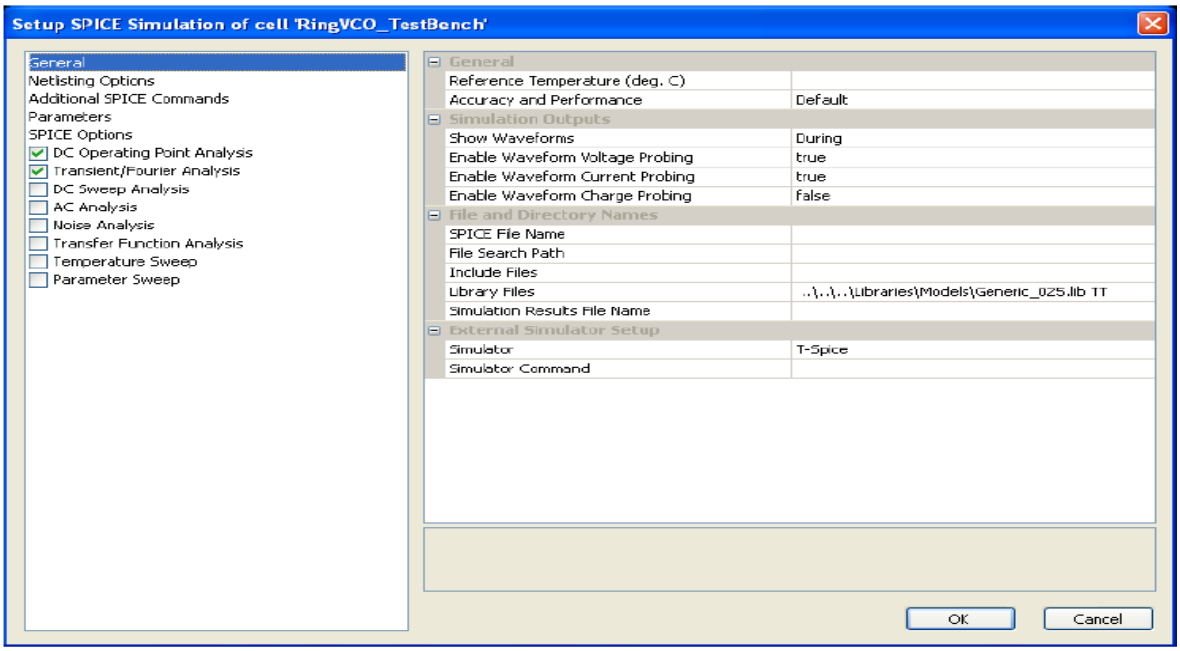
Including Spice Commands and Checking Waveform

28. Now include SPICE_commands (print voltage) from library & Connect this to input and output port to check waveform
29. Include model file (hp05.md) with SPICE_commands -> include Hp05.md file location is inserted as shown below:
    "Specific folder where Examples and tutorial was installed during set up\Tanner EDA\Tanner Tools v13.0\L-Edit and LVS\LVS\SPR_Core\hp05.md"
    Note: Tutorial and example files may be installed at any time by invoking Help > Setup Examples and Tutorial from S-Edit, or by invoking Setup Examples and Tutorial from the Windows start menu for S-Edit. Modified tutorial files Can be replaced with a fresh copy of the tutorial files by invoking Help > Setup Examples and Tutorial, and choosing Repair, when asked to select from the options Modify, Repair, and Remove.
30. Paste this include command anywhere at workspace.

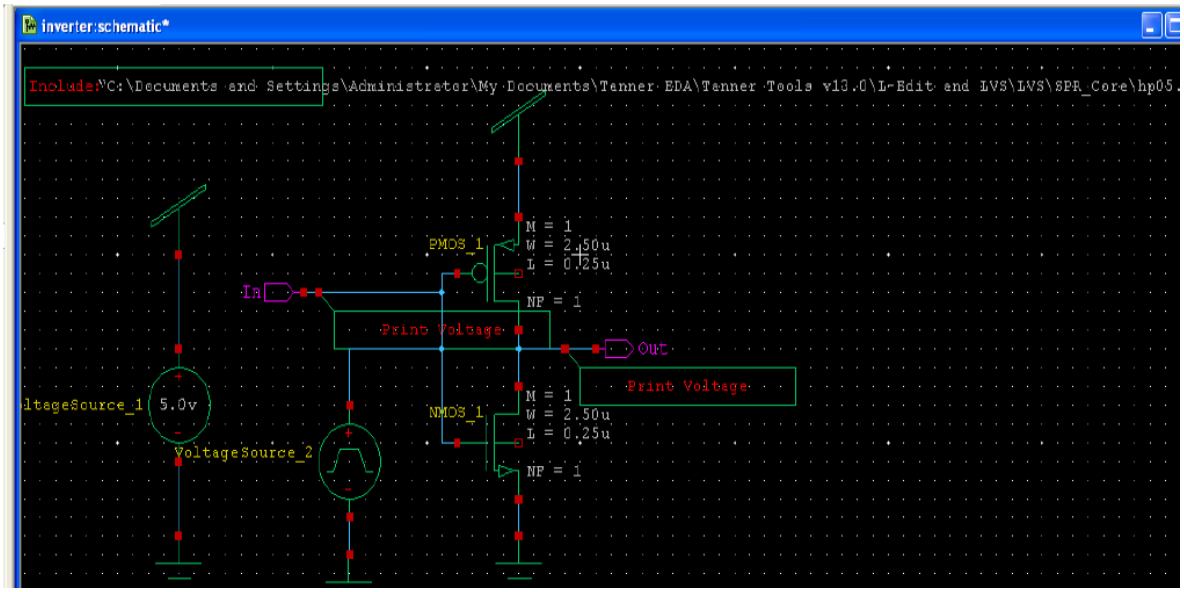
31. Now circuit is complete. Just save it. You can follow different saving options given below.
    There are four ways of saving a file:
    - **File > Save > Save Design.** *Design Name* saves modifications to the design, but does not save modifications to any libraries.
    - **File > Save > Save Design.** *Design Name* **and Its Libraries** saves modifications to the design and all libraries.
    - **File > Save > Save** *# Selected* **Design/Libraries** saves those Design/Libraries that are selected in the list of libraries in the Library browser.
    - The **Save Copy of …** command saves a copy of the selected Design and Libraries in the Library Browser to a new location on disk. The Save Copy of … command is not the same as a Save As command in that after the command is issued, the application is still editing the original design, not the newly saved design.

Simulating the Design
SPICE simulation using the T-Spice engine

32. For simulation of design go to Setup-> Spice Simulation



33. Select Spice options (Eg. DC Operating Point Analysis and/or Transient Analysis) then define time and other parameters. Press OK in the **Simulation Setup** dialog.
34. Select Tools-> start simulation or press the Simulate button, ( ), to run the simulation. It will follow Procedure 1 given in T-Spice demonstration. Go to the next page.



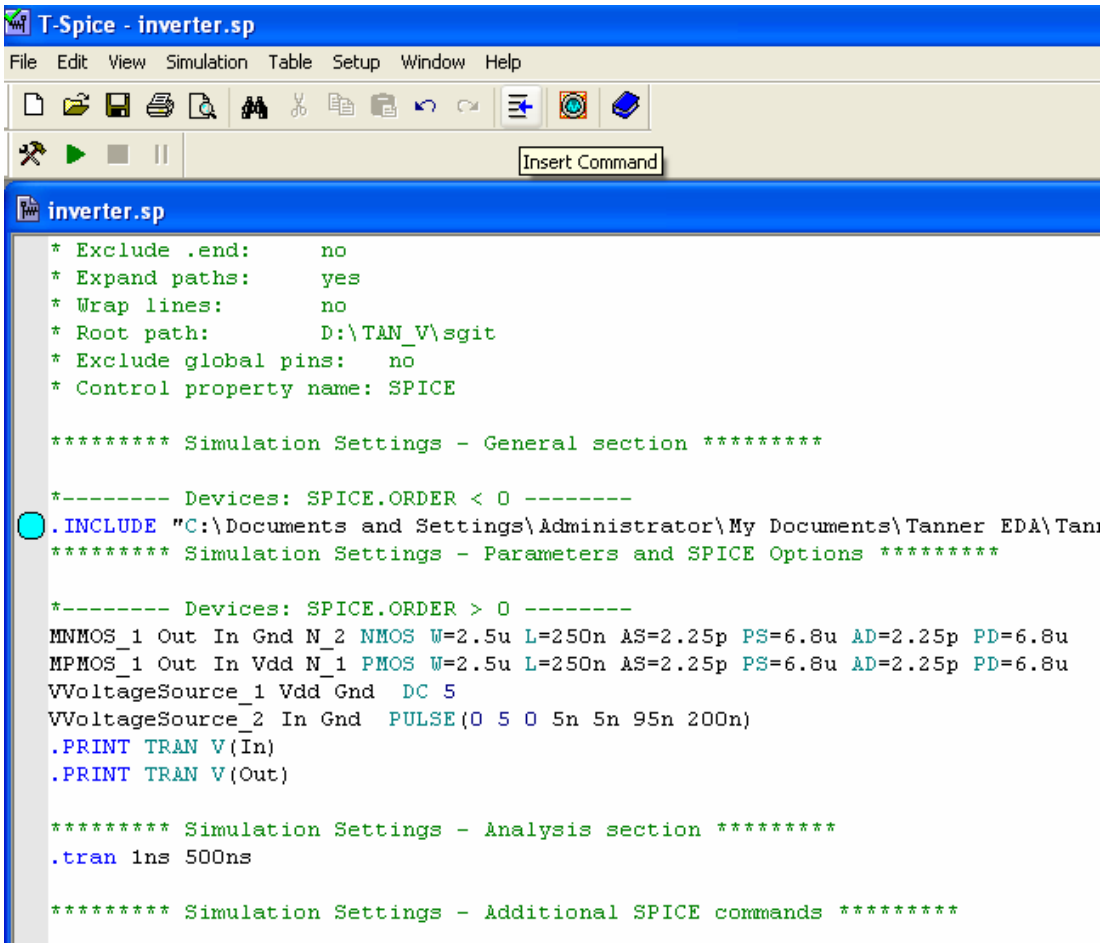
T-SPICE

Procedure 1:

Running simulation in S-Edit will automatically invoke T-Spice software. Waveform appears in W-Edit window directly.

Procedure 2:

1. If Steps 28-30 are not followed earlier then click on T-Spice icon ***[T]*** in S-Edit window. A Netlist file will be open with extension **.sp**. Place the cursor at the beginning of the next blank line. Invoke **Edit > Insert Command** (shortcut **Ctrl+M** or use the toolbar icon) to open the *Command Tool*. Insert desired Spice commands. To include model file specify the path "Specific folder where Examples and tutorial was installed during set up\Tanner EDA\Tanner Tools v14.1\L-Edit and LVS\LVS\SPR_Core\hp05.md". Insert also the output commands as per requirement. For an example a T-Spice netlist file is given below.
2. Then simulation -> run simulation or click on simulation icon. T-Spice will automatically invoke W-Edit.



W-EDIT

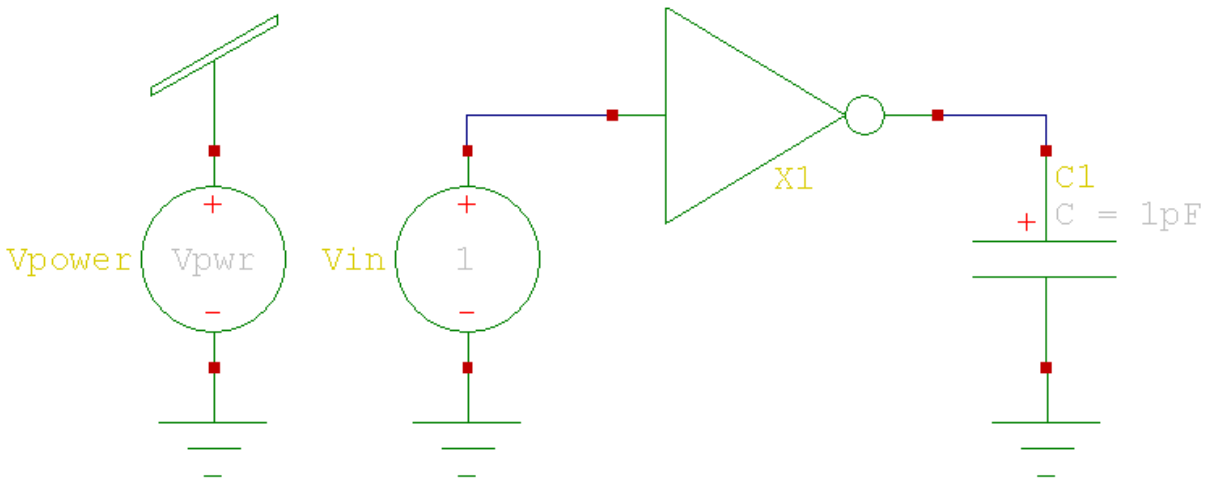
Waveform can be checked using W-Edit. It will automatically invoke at the time of running T-spice. Results will appear in W-Edit, displaying the voltage waveforms for the nodes indicated with the Print Voltage commands or commands inserted in the netlist file.

CHAPTER 2: DC OPERATING POINT ANALYSIS

DC operating point analysis finds a circuit's steady-state condition, obtained (in principle) after the input voltages have been applied for an infinite amount of time.

Schematic	...\Tanner EDA\Tanner Tools v12.6\T-Spice\Analysis Examples\ **Inverter_TestBench Operating Point**
T-Spice Input	...\Tanner EDA\Tanner Tools v12.6\T-Spice\Simulation Results\ **Inverter OP.sp**
Output	...\Tanner EDA\Tanner Tools v12.6\T-Spice\Simulation Results\ **Inverter OP.out**

Schematic



(This CMOS inverter is also used in *Example 2: DC Transfer Analysis* and *Example 3: Transient Analysis—Inverter*.)

Each of the components visible in the schematic has properties associated with it. Properties are textual elements, created in DxDesigner, that are attached to an object and provide key information about its design and simulation commands in T-Spice.

If you "push in" to open a specific instance, you can see that the physical dimensions of the component **N1** in the inverter are defined by the properties:

M = 1
W = 2.5u
L = 0.25u

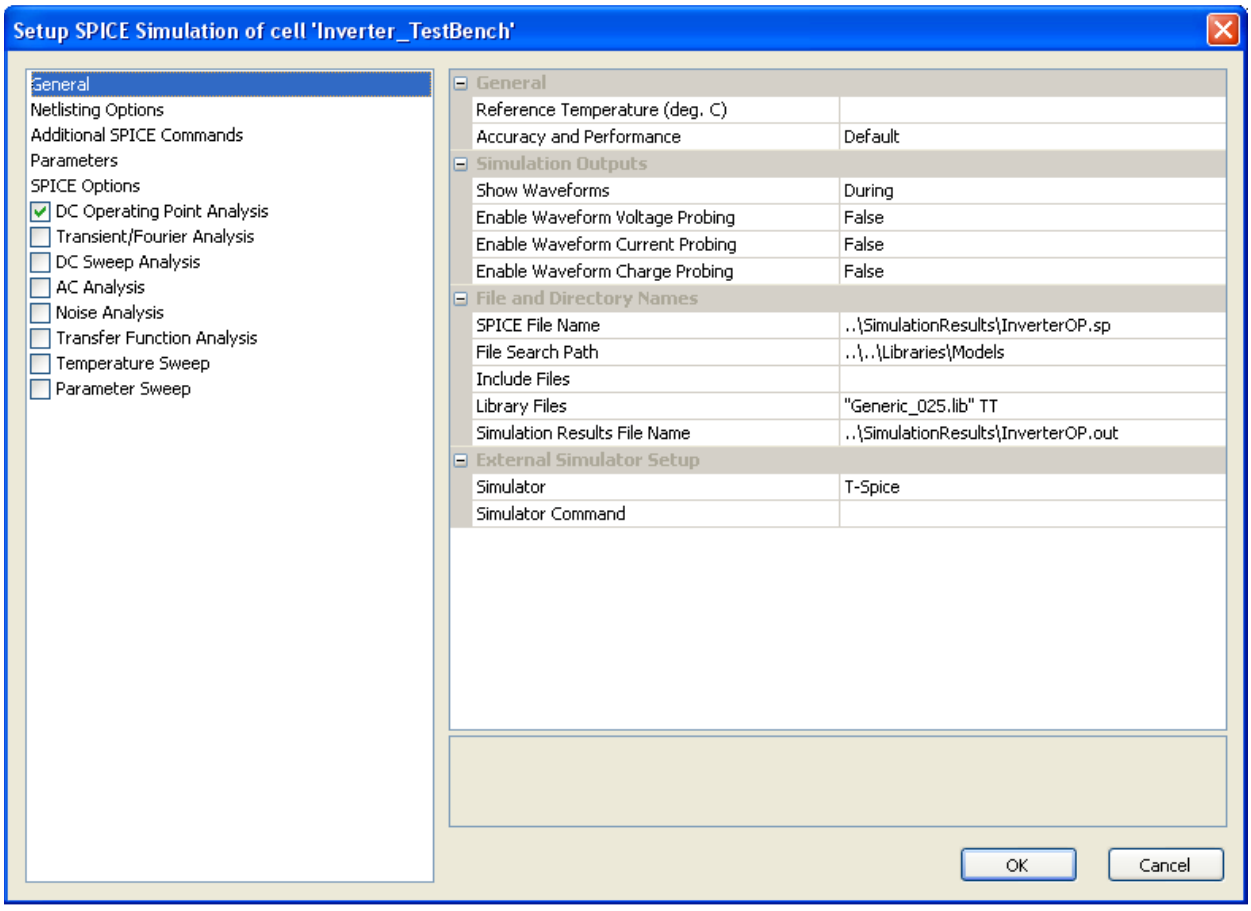
N1 is an instance of the symbol **NMOS**, which represents an *n*-channel MOSFET transistor. Properties that describe the operation of a generic *n*-channel MOSFET are defined at the symbol level. Properties specific to component **N1**, such as length and width, are defined when **N1** is created. Property values defined at the component level take precedence over default (symbol) values.

SPICE Simulation Setup in S-Edit

Prior to running the T-Spice simulation, the analysis commands and all processing options need to be established. This is accomplished using the **Setup SPICE Simulation** dialog in DxDesigner.

 Ensure that you are viewing the top level schematic. For this example, the top level cell is named **inverter_TestBench OperatingPoint**. Right-click on **inverter_TestBench** in the **Libraries** window and use **Open View** to select the schematic **OperatingPoint**.

 Use **Setup > SPICE Simulation** to launch the **Setup SPICE Simulation** dialog. The proper simulation settings for the **Inverter_TestBench** example have already been entered for you. Note that the **DC Operating Point Analysis** box is checked. Also note the settings in the **General** options for **File Search Path** and **Include Files**.



Export the Netlist to T-Spice

 In the **inverter_Testbench Operating Point** schematic, use **Tools > Design Checks** to execute the **Design Checker**.

 The **Design Checker** will display any violation or errors in the **Command** window. There should not be any errors in the file **inverter_Testbench Operating Point**.

 Press the T-Spice icon ( ) to export a T-Spice netlist file named **inverterOP.sp**. DxDesigner will launch T-Spice with the **inverterOP.sp** netlist open.

T-Spice Input

********* Simulation Settings - General section *********
.option search="C:\src\TannerToolsShippingFiles\Libraries\Models"
.lib "Generic_025.lib" TT

*-------- Devices: SPICE.ORDER < 0 --------
* Design: AnalysisExamples / Cell: Inverter_TestBench / View: OperatingPoint
/ Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: Operating point analysis testbench of an inverter
* Date: 06/15/2007 2:56:17 PM
* Revision: 0

********** Subcircuits **********
.subckt INV A Out Gnd Vdd
*-------- Devices: SPICE.ORDER < 0 --------
* Design: LogicGates / Cell: INV / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: Inverter
* Date: 06/15/2007 2:56:17 PM
* Revision: 0

*-------- Devices: SPICE.ORDER == 0 --------
MP1 Out A Vdd Vdd PMOS W=2.5u L=250n M=2 AS=4.5p PS=13.6u AD=3.125p PD=7.5u
MN1 Out A Gnd 0 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
.ends

********* Simulation Settings - Parameters and SPICE Options *********
.param Vpwr = 3.3v
*-------- Devices: SPICE.ORDER == 0 --------
VVin N_2 Gnd DC 1
XX1 N_2 N_1 Gnd Vdd INV
VVpower Vdd Gnd DC Vpwr
CC1 N_1 Gnd 1p

********* Simulation Settings - Analysis section *********
.op

********* Simulation Settings - Additional SPICE commands *********

.end

Two transistors, **MP1** and **MN1**, are defined in **inverterOP.sp**. These are MOSFETs, as indicated by the key letter **M** that begins their names. Following each transistor name are the names of its terminals in the required order: drain–gate–source–bulk. Then the model name (**PMOS** or **NMOS** in this example) and physical characteristics, such as length and width, are specified.

A capacitor **CC1** (signified by the key letter **C**) connects nodes **N 1** and **GND** with a capacitance of 1p. (Strictly speaking, the capacitor could be omitted from the circuit for this example, since it does not affect the DC operation of the inverter.)

Two DC voltage sources are defined: **VVin**, which sets node **N2** to 1.0 volt relative to ground and **VVpower**, which sets node **Vdd** to 3.3 volts as defined by the variable **Vpwr**.

 Notice that the simulation settings which were entered in the **SPICE Simulation Setup** dialog resulted in **.option**, **.lib,** and **.op** commands being written to the T-Spice input file. The **.lib** command causes T-Spice to read the contents of the **Generic_025.lib** library file for the evaluation of transistors **MP1** and **MN1**, and the **search** option identifies the path to the library files. In this case, the library file contains two device **.model** commands, describing MOSFET models **PMOS** and **NMOS**, as shown below for
PMOS:

+VERSION = 3.1 TNOM = 27 TOX = 5.6E-9
+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.4935548
+K1 = 0.6143278 K2 = 6.804492E-4 K3 = 0
+K3B = 5.8844074 W0 = 1E-6 NLX = 6.938169E-9
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.3578746 DVT1 = 0.7014778 DVT2 = -0.1881376
+U0 = 100 UA = 9.119231E-10 UB = 1E-21
+UC = -1E-10 VSAT = 1.782051E5 A0 = 0.9704347
+AGS = 0.1073973 B0 = 2.773991E-7 B1 = 8.423987E-7
+KETA = 0.0104811 A1 = 0.0193128 A2 = 0.3
+RDSW = 694.5830247 PRWG = 0.3169639 PRWB = -0.1958978
+WR = 1 WINT = 0 LINT = 2.971337E-8
+XL = 0 XW = -4E-8 DWG = -2.967296E-8
+DWB = -2.31786E-10 VOFF = -0.1152095 NFACTOR = 1.1064678
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.3676411 ETAB = -0.0915241
+DSUB = 1.1089801 PCLM = 1.3226289 PDIBLC1 = 9.913816E-3
+PDIBLC2 = -1.499968E-6 PDIBLCB = -1E-3 DROUT = 0.1276027
+PSCBE1 = 8E10 PSCBE2 = 5.772776E-10 PVAG = 0.0135936

```
+DELTA = 0.01          RSH = 3            MOBMOD = 1
+PRT = 0               UTE = -1.5         KT1 = -0.11
+KT1L = 0              KT2 = 0.022        UA1 = 4.31E-9
+UB1 = -7.61E-18       UC1 = -5.6E-11     AT = 3.3E4
+WL = 0                WLN = 1            WW = 0
+WWN = 1               WWL = 0            LL = 0
+LLN = 1               LW = 0             LWN = 1
+LWL = 0               CAPMOD = 2         XPART = 0.5
+CGDO = 5.59E-10       CGSO = 5.59E-10    CGBO = 5E-10
+CJ = 1.857995E-3      PB = 0.9771691     MJ = 0.4686434
+CJSW = 3.426642E-10   PBSW = 0.871788    MJSW = 0.3314778
+CJSWG = 2.5E-10       PBSWG = 0.871788   MJSWG = 0.3314778
+CF = 0                PVTH0 = 4.137981E-3  PRDSW = 7.2931065
+PK2 = 2.600307E-3     WKETA = 0.0192532  LKETA = -5.972879E-3
)
```

Generic_025.lib assigns values to various Level 49 MOSFET model parameters for both *n*- and *p*channel devices. T-Spice uses these parameters to evaluate Level 49 MOSFET model equations.

The **.op** command performs a DC operating point calculation and writes the results to the file specified in the **Simulation > Run Simulation** dialog.

Run the Simulation In T-Spice

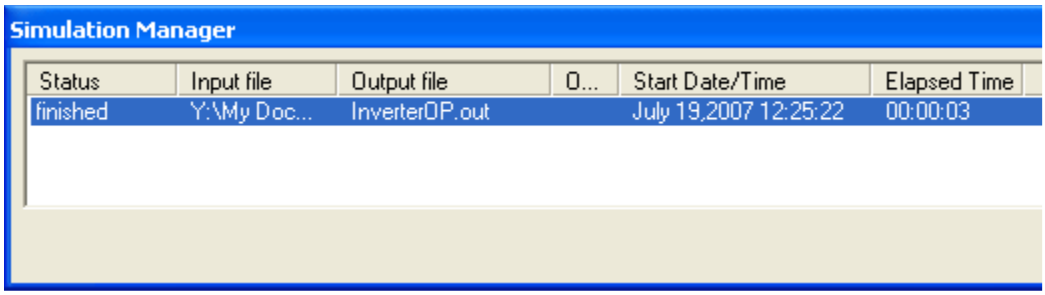
 With **inverterOP.sp** open in T-Spice, use **File > Save** to save the file.
 Click the **Run Simulation** button ( ) in the T-Spice simulation toolbar.
 In the **Run Simulation** dialog, click **Start Simulation**.
 T-Spice will open a new window displaying the simulation log.

Output

The output file lists the DC operating point information for the circuit. You can read this file in T-Spice
or any text editor.

Open the Output File

 If not already displayed, select **View > Simulation Manager** from the T-Spice menu to open the
Simulation Manager:



 Select the **InverterOP.out** display line in the window, then click the **Show Output** button to open the output file **InverterOP.out** in a new T-Spice window.

 If you prefer to view the output in a text editor, simply open **InverterOP.out** as a text file. (It is located in the same directory as the input file.)

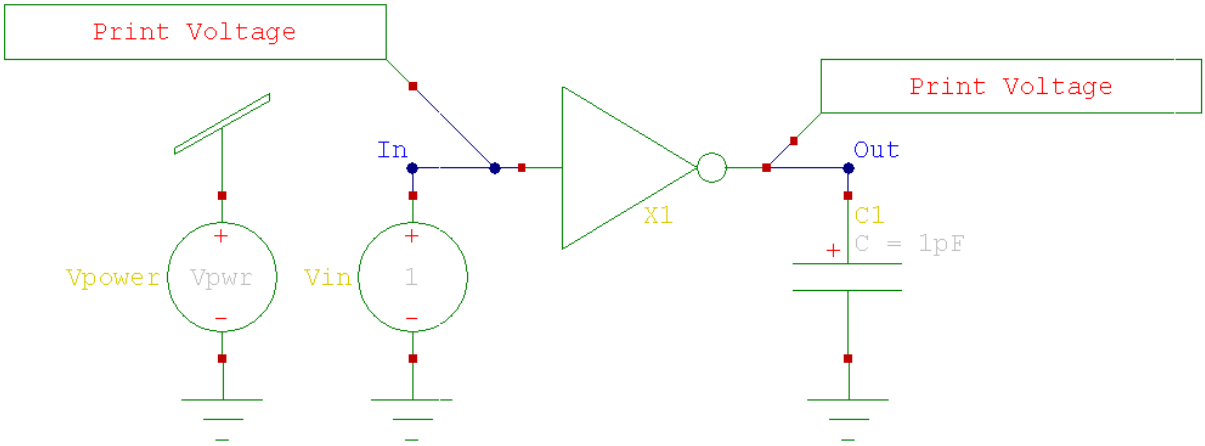
 The output file contains the following DC operating point information (in addition to comments of various kinds, not shown here. (You can also view DC operating voltages, currents and small-signal parameters in S-Edit.)

DC ANALYSIS - temperature=25.0
v(N_1) = 3.0633e+000
v(N_2) = 1.0000e+000
v(Vdd) = 3.3000e+000
i1(VVin) = 0.0000e+000
i2(VVin) = 0.0000e+000
i1(VVpower) = -3.1508e-004
i2(VVpower) = 3.1508e-004

CHAPTER 3: DC TRANSFER ANALYSIS

DC transfer analysis is used to study the voltage or current at one set of points in a circuit as a function of the voltage or current at another set of points. This is done by *sweeping* the source variables over specified ranges and recording the output.

Schematic



This schematic includes a **.print** command, which measures and records voltages at the input and output nodes of the circuit. The command is contained within the **DC analysis output** cell.

T-Spice Input

If T-Spice is open when you run the simulation in S-Edit, the SPICE file **inverterDC.sp** will open and run automatically.

********* Simulation Settings - General section *********
.option search="...\Tanner EDA\Tanner Tools v12.6\Libraries\Models"
.probe
.option probev
.lib "Generic_025.lib" TT
*-------- Devices: SPICE.ORDER < 0 --------
* Design: AnalysisExamples / Cell: Inverter_TestBench / View: DCAnalysis /
Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: DC analysis testbench of an inverter
* Date: 06/15/2007 2:56:17 PM

* Revision: 0
********** Subcircuits **********

```
.subckt INV A Out Gnd Vdd

*-------- Devices: SPICE.ORDER < 0 --------

* Design: LogicGates / Cell: INV / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: Inverter
* Date: 06/15/2007 2:56:17 PM
* Revision: 0

*-------- Devices: SPICE.ORDER == 0 --------

MP1 Out A Vdd Vdd PMOS W=2.5u L=250n M=2 AS=4.5p PS=13.6u AD=3.125p PD=7.5u
MN1 Out A Gnd 0 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
.ends
‘
********* Simulation Settings - Parameters and SPICE Options *********

.param Vpwr = 3.3v

*-------- Devices: SPICE.ORDER == 0 --------

VVin In Gnd DC 1
XX1 In Out Gnd Vdd INV
VVpower Vdd Gnd DC Vpwr
CC1 Out Gnd 1p

*-------- Devices: SPICE.ORDER > 0 --------
.
PRINT DC V(Out)
.PRINT DC V(In)

********* Simulation Settings - Analysis section *********

.dc lin VVin 0.0 3.3 0.02 lin VVpower 2.3 4.3 0.5

********* Simulation Settings - Additional SPICE commands *********

.end
```

The **.DC** command, indicating transfer analysis, is followed by the parameter **lin**, which specifies a linear sweep. Next is a list of sources to be swept, and the voltage ranges across which the sweeps are to take place.

In this example, **VVin** will be swept from 0 to 3.3 volts in 0.02 volt increments, and **VVpower** will be swept from 2.3 to 4.3 volts in 0.5 volt increments.

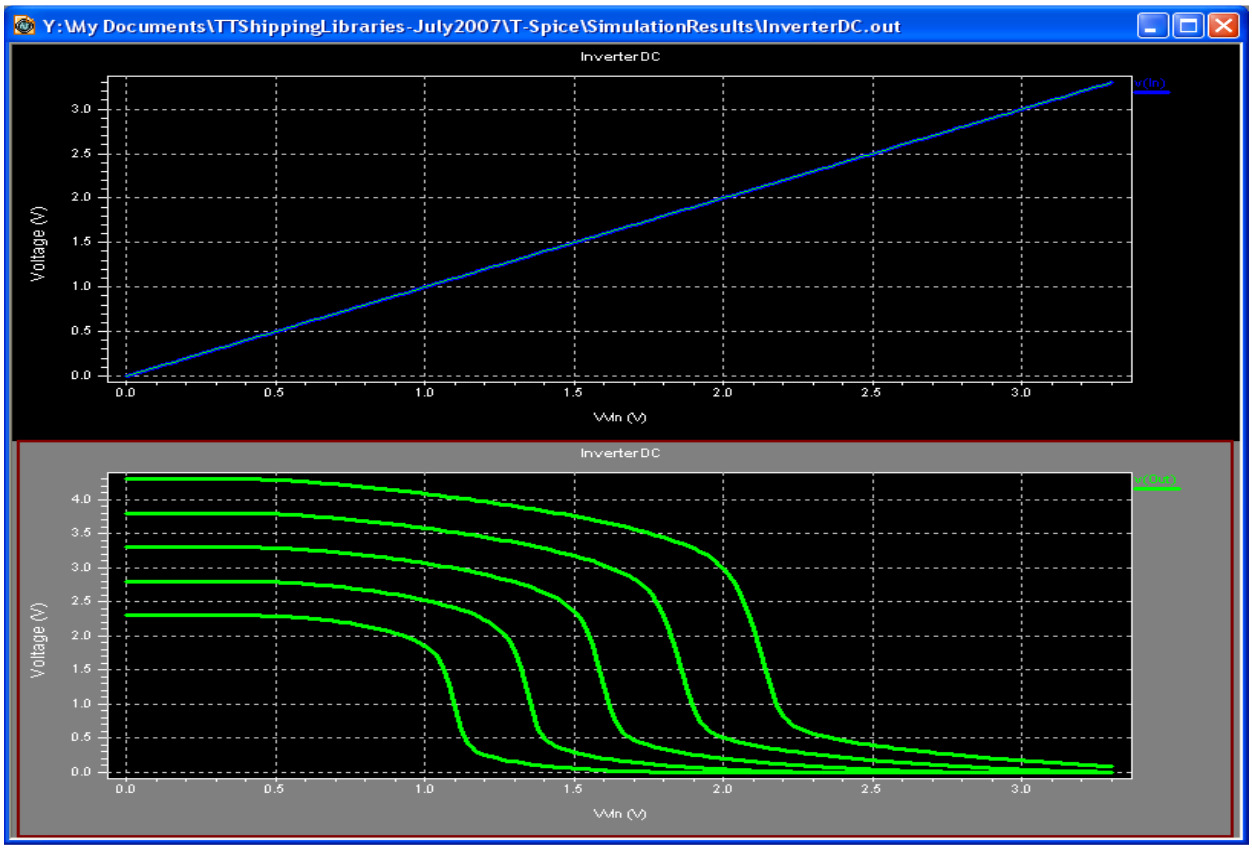
The transfer analysis will be performed as follows: **VVpower** will be set at 2.3 volts and **V1** will be swept over its specified range; **VVpower** will then be incremented to 2.5 volts and **V1** will be reswept over its range; and so on, until **VVpower** reaches the upper limit of its range.

The **.DC** command ignores the values assigned to the voltage sources **VVpower** and **VVin** in the voltage source statements; however, they must be declared in those statements.

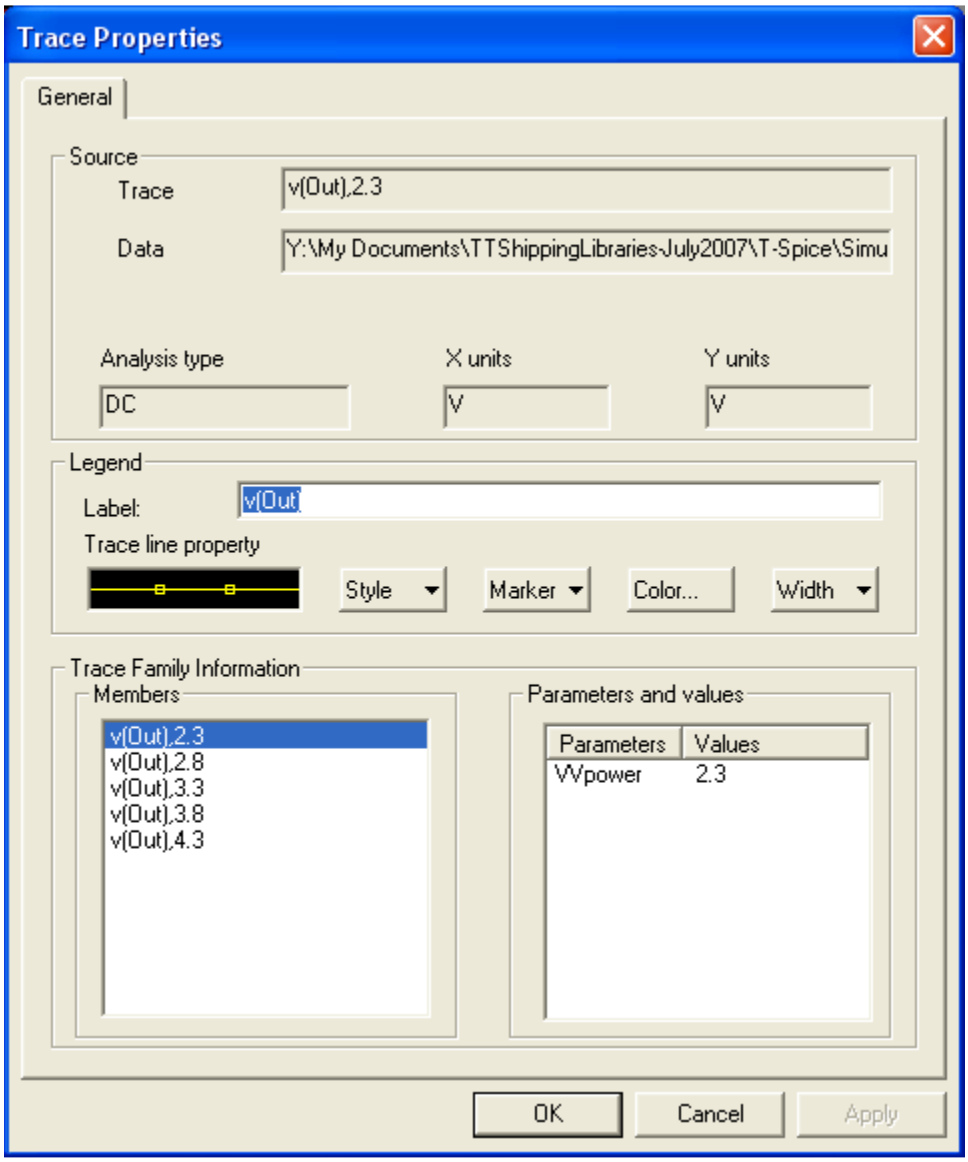
The resulting voltages for nodes **IN** and **OUT** are reported by the **.PRINT DC** command to the specified destination.

Output

When W-Edit launches, simulation results of the same data type, which in this case is voltage, are automatically plotted on a single chart. In this example, traces were separated into different charts and reorganized (according to data type) using the commands in **Chart > Expand Chart** of the W-Edit menu.
The charts below show input and output voltages to the circuit, with separate traces for each sweep of **v(Out)**. To view detailed information about a trace, double-click on the trace or on the trace label located in the upper right corner of the chart.



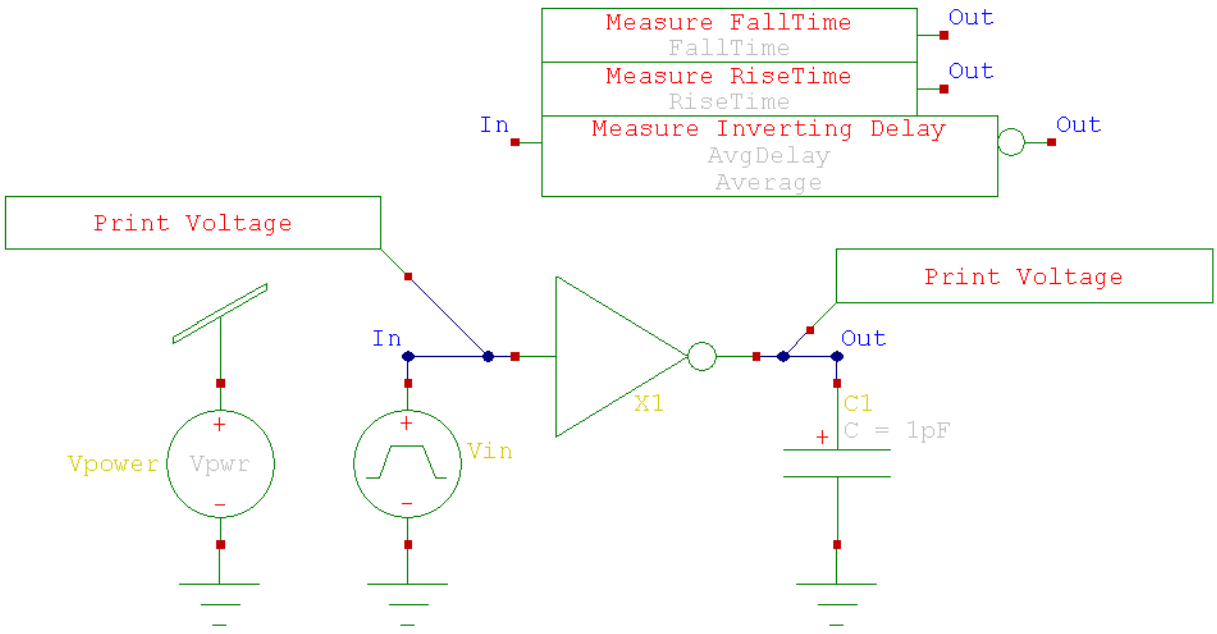
The **Trace Properties** dialog displays the value of parameter **v(Out)** corresponding to each trace, as well as labels and line properties.



CHAPTER 4: TRANSIENT ANALYSIS—INVERTER

Transient analysis provides information on how circuit elements vary with time.
The basic T-Spice command for transient analysis has three modes. In the *op* mode (default), the DC operating point is computed, and T-Spice uses this as the starting point for the transient simulation.

Schematic



T-Spice Input

********* Simulation Settings - General section *********
.option search="...\Tanner EDA\Tanner Tools v12.6\Libraries\Models"
.probe
.option probev
.option probei
.lib "Generic_025.lib" TT

*-------- Devices: SPICE.ORDER < 0 --------

* Design: AnalysisExamples / Cell: Inverter_TestBench / View:
TransientAnalysis / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.

```
* Info: Transient analysis testbench of an inverter
* Date: 12/18/2005 7:28:14 PM
* Revision: 5

********** Subcircuits **********

.subckt INV A Out Gnd Vdd
*-------- Devices: SPICE.ORDER < 0 --------
* Design: LogicGates / Cell: INV / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: Inverter
* Date: 12/18/2005 7:28:14 PM
* Revision: 5

*-------- Devices: SPICE.ORDER == 0 --------

MP1 Out A Vdd Vdd PMOS W=2.5u L=250n M=2 AS=4.5p PS=13.6u AD=3.125p PD=7.5u
MN1 Out A Gnd 0 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
.ends

********* Simulation Settings - Parameters and SPICE Options *********

.param Vpwr = 3.3v

*-------- Devices: SPICE.ORDER == 0 --------

VVin In Gnd PULSE(0 Vpwr 0 1n 1n 49n 100n)
XX1 In Out Gnd Vdd INV
VVpower Vdd Gnd DC Vpwr
CC1 Out Gnd 1p

*-------- Devices: SPICE.ORDER > 0 --------

.PRINT TRAN V(Out)
.PRINT TRAN V(In)
.MEASURE TRAN RiseDelay_MeasureDelay_1 TRIG v(In) VAL='(Vpwr-0)*50/100+0'
TD='0' RISE=1 TARG v(Out) VAL='(Vpwr-0)*50/100+0' TD='0' FALL=1 OFF
.MEASURE TRAN FallDelay_MeasureDelay_1 TRIG v(In) VAL='(Vpwr-0)*50/100+0'
TD='0' FALL=1 TARG v(Out) VAL='(Vpwr-0)*50/100+0' TD='0' RISE=1 OFF
.MEASURE TRAN AvgDelay
PARAM='(RiseDelay_MeasureDelay_1+FallDelay_MeasureDelay_1)/2.0' ON
.MEASURE TRAN FallTime TRIG v(Out) VAL='(Vpwr-0)*90/100+0' TD=0 Fall=1 TARG
v(Out) VAL='(Vpwr-0)*10/100+0' TD=0 FALL=1 ON
.MEASURE TRAN RiseTime TRIG v(Out) VAL='(Vpwr-0)*10/100+0' TD=0 RISE=1 TARG
v(Out) VAL='(Vpwr-0)*90/100+0' TD=0 RISE=1 ON
```

********* Simulation Settings - Analysis section *********

.tran 250p 300n

********* Simulation Settings - Additional SPICE commands *********

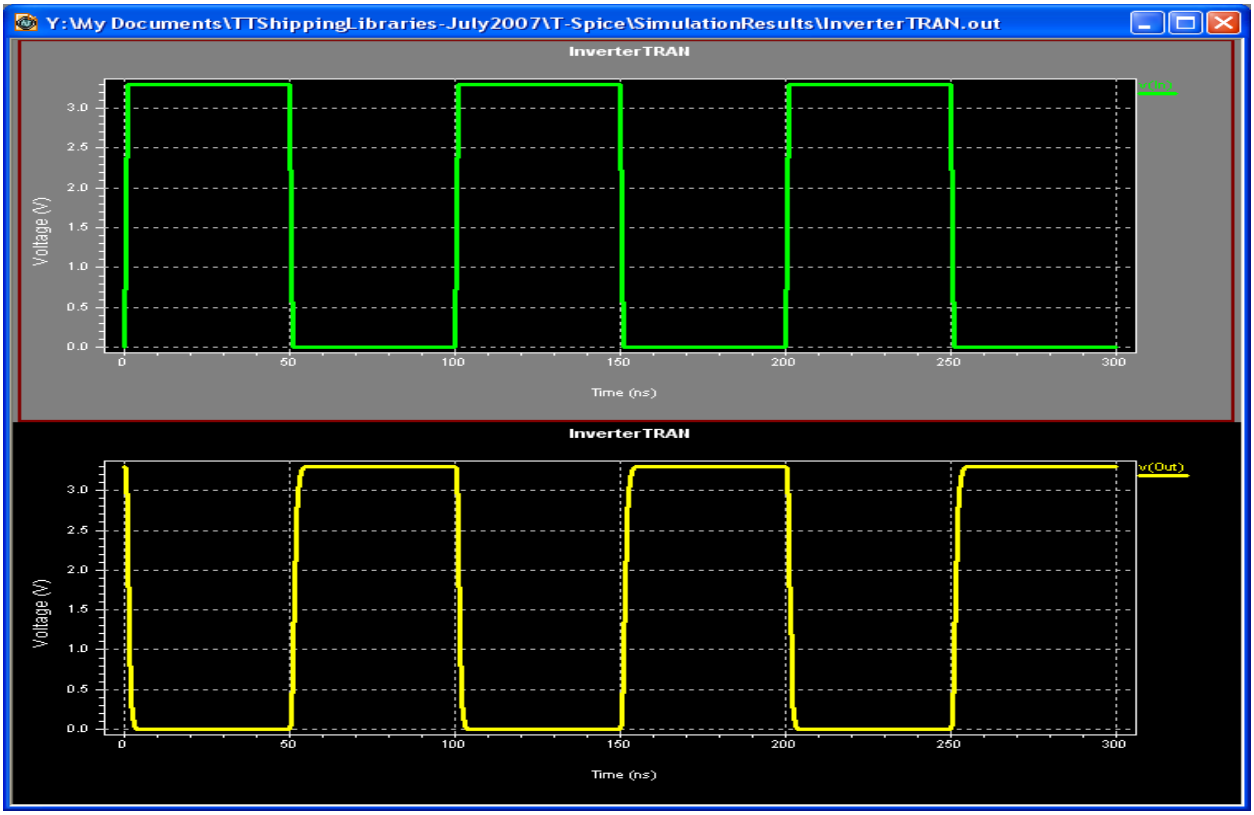
.end

This circuit is similar to that of chapter 1, except that voltage source **VVin** here generates a pulse (indicated by the keyword **pulse**) to **In**, rather than setting a constant value.

The times and voltages that define the "legs" of the waveform are specified in the arguments to **pulse**.The initial current is zero amperes and the peak current is **Vpwr**, with an initial delay of zero seconds.The rise and fall times are one nanosecond, with a pulse width of 49 nanoseconds and a pulse period of100 nanoseconds.

The **.tran** command specifies the characteristices of the transient analysis to be performed; in this example the maximum time step allowed is 250 pico with a total duration of 300 nanoseconds.

Output



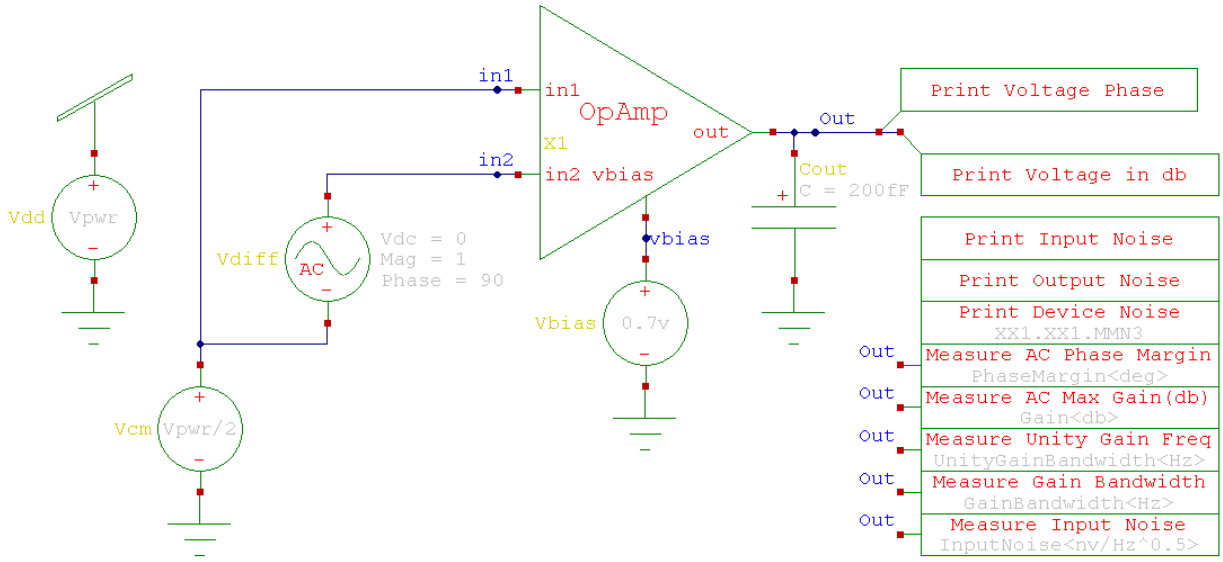
CHAPTER 5: AC ANALYSIS

AC analysis characterizes the circuit's behavior dependence on small-signal input frequency. It involves three steps:

(1) Calculating the DC operating point;
(2) Linearizing the circuit; and
(3) solving the linearized circuit for each frequency.

This example involves a standard operational amplifier, consisting of one PMOS, one NMOS, a transconductance amplifier and one capacitor.

Schematic



T-Spice Input

********* Simulation Settings - General section *********
.option Accurate
.option search="...\Tanner EDA\Tanner Tools v12.6\Libraries\Models"
.probe
.option probev
.option probei
.lib "Generic_025.lib" TT

********** Subcircuits **********

.subckt TransAmp in1 in2 out vbias Gnd Vdd

```
*-------- Devices: SPICE.ORDER < 0 --------

* Design: AnalysisExamples / Cell: TransAmp / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.

* Info: Transconductance Amplifier
* Date: 06/15/2007 2:56:17 PM
* Revision: 0

*-------- Devices: SPICE.ORDER == 0 --------

MMP1 vm1 vm1 Vdd Vdd PMOS W=2u L=2u AS=1.8p PS=5.8u AD=1.8p PD=5.8u
MMP2 out vm1 Vdd Vdd PMOS W=2u L=2u AS=1.8p PS=5.8u AD=1.8p PD=5.8u
MMN1 vm1 in1 vn1 0 NMOS W=2u L=2u AS=1.8p PS=5.8u AD=1.8p PD=5.8u
MMN2 out in2 vn1 0 NMOS W=2u L=2u AS=1.8p PS=5.8u AD=1.8p PD=5.8u
MMN3 vn1 vbias Gnd 0 NMOS W=2u L=3u AS=1.8p PS=5.8u AD=1.8p PD=5.8u
.ends
...
*-------- Devices: SPICE.ORDER == 0 --------
XX1 in1 in2 vf1 vbias Gnd Vdd TransAmp
MMP1 Out vf1 Vdd Vdd PMOS W=6u L=2u AS=5.4p PS=13.8u AD=5.4p PD=13.8u
CComp vf1 Out 200f
MMN1 Out vbias Gnd 0 NMOS W=3u L=2u AS=2.7p PS=7.8u AD=2.7p PD=7.8u
.ends

********* Simulation Settings - Parameters and SPICE Options *********

.param Vpwr = 3.3v
*-------- Devices: SPICE.ORDER == 0 --------
VVdd Vdd Gnd DC Vpwr
VVdiff in2 in1 DC 0 AC 1 90
VVcm in1 Gnd DC Vpwr/2
VVbias vbias Gnd DC 700m
CCout Out Gnd 200f
XX1 Out in1 in2 vbias Gnd Vdd OpAmp

*-------- Devices: SPICE.ORDER > 0 --------

.PRINT AC Vdb(Out)
.PRINT AC Vp(Out)
.PRINT NOISE INOISE
.PRINT NOISE ONOISE
.PRINT NOISE TRANSFER dn(XX1.XX1.MMN3)
.MEASURE NOISE InputNoise<nv/Hz^0.5> FIND 'inoise/1E-9' WHEN Vdb(Out)=0 ON
.MEASURE AC UnityGainBandwidth<Hz> WHEN Vdb(Out)=0 ON
.MEASURE AC MeasureGainBandwidthProduct_1_Gain MAX vdb(Out) OFF
```

```
.MEASURE AC MeasureGainBandwidthProduct_1_UGFreq WHEN Vdb(Out)=0 OFF
.MEASURE AC GainBandwidth<Hz>
PARAM='MeasureGainBandwidthProduct_1_Gain*MeasureGainBandwidthProduct_1_U
GFreq' ON
.MEASURE AC Gain<db> MAX vdb(Out) ON
.MEASURE AC PhaseMargin<deg> FIND '90+vp(Out)' WHEN vdb(Out)=0 ON

********* Simulation Settings - Analysis section *********
.op
.ac dec 10 1 100Meg
.noise v(Out) VVdiff 5
```

Three voltage sources (in addition to **Vdd**) are defined.

 Vdiff sets the DC voltage difference between nodes **IN2** and **IN1** to 0 volts; the AC magnitude is 1 volt and its AC phase is 90 degrees.

 Vcm sets node **IN1** to 2 volts, relative to **GND**.

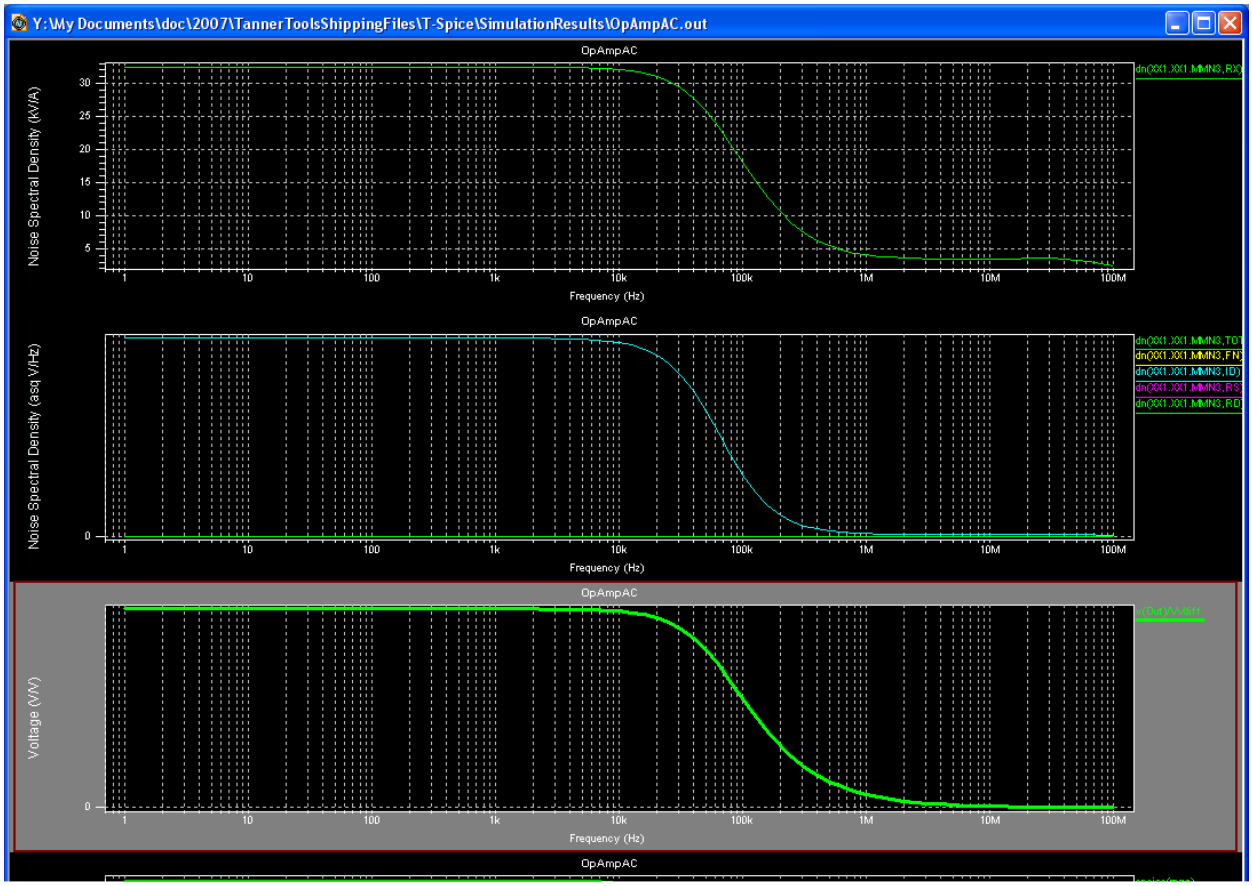
 Vbias sets node **vbias** to 700 mille volts, relative to **GND**.

The **.ac** command performs an AC analysis. Following the **.ac** keyword is information concerning the frequencies to be swept during the analysis. In this case, the frequency is swept logarithmically, by decades (**DEC**); 10 data points are to be included per decade; the starting frequency is 1 Hz and the ending frequency is 100 MHz.

The **.PRINT** command writes the voltage magnitude (in decibels) and phase (in degrees), respectively, for the node **OUT** to the specified file.

Output

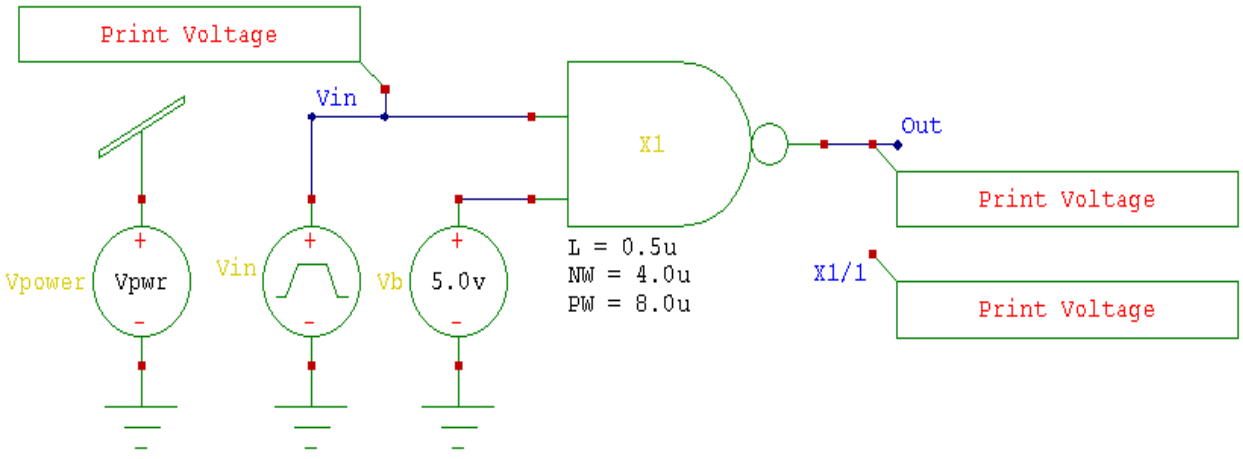
The AC simulation will result in **AC** small-signal model parameters being written to the output file, in addition to all output generated from the **.print** statements.


Y:\My Documents\doc\2007\TannerToolsShippingFiles\T-Spice\SimulationResults\OpAmpAC.out
OpAmpAC
Noise Spectral Density (nV/A)
Frequency (Hz)
OpAmpAC
Noise Spectral Density (asq V/Hz)
Frequency (Hz)
OpAmpAC
Voltage (V/V)
Frequency (Hz)
OpAmpAC

CHAPTER 6: USING SUB-CIRCUITS

Subcircuit definitions allow arbitrarily complex arrangements of nodes and devices to be easily reused multiple times in a circuit. A subcircuit definition in DxDesigner is contained within a cell definition, and is comprised of both a schematic view and a symbol view. Each instance of the symbol encapsulates the subcircuit schematic, allowing a simple but complete representation of subcircuit dynamics.
This example uses a NAND gate to illustrate the use of subcircuit definitions and subcircuit parameters.

Schematic



An instance of the subcircuit **NAND** is created in the schematic and labeled **X1**. (To access **NAND** from the main schematic, double-click on the **NAND** item in the Libraries list.)

As discussed in chapter 2, symbol properties are used to define component properties such as length and width. This example introduces a new symbol property, SPICE.PARAMETER, which allows parameters to be passed through a hierarchical netlist.

The symbol that represents NAND has the SPICE parameter property **L=NW=PW=** which specifies that the cell properties L, NW, and PW are subcircuit parameters of NAND. The cell also contains the three property definitions L = 0.5u, NW = 4.0u, and PW = 8.0u.
These parameters define properties of all *n*-channel and *p*-channel MOSFETS within the subcircuit such that **L** represents the length property of both *n*- and *p*-channel MOSFETS, **NW** represents *n*-channel width and **PW** represents *p*-channel width.

Attaching these parameters to **NAND** allows component properties within the subcircuit definition to be controlled in the subcircuit call.

T-Spice Input

```
********* Simulation Settings - General section *********
.option search="...\Tanner EDA\Tanner Tools v12.6\Libraries\Models"
.probe
.option probev
.option probei
.lib "Generic_025.lib" TT
*-------- Devices: SPICE.ORDER < 0 --------
* Design: AnalysisExamples / Cell: Subcircuit_TestBench / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: Testbench for subcircuit example
* Date: 7/13/2007 7:59:21 AM
* Revision: 19

*************** Subcircuits *****************

.subckt NAND A B Out Gnd Vdd L=500n NW=4u PW=8u
*-------- Devices: SPICE.ORDER < 0 --------
* Design: AnalysisExamples / Cell: NAND / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: 2 input NAND gate
* Date: 7/13/2007 7:59:21 AM
* Revision: 95

*-------- Devices: SPICE.ORDER == 0 --------

MP1 Out A Vdd Vdd PMOS W=PW L=L M=2 AS='if(0,
(900n*PW+floor(2/2)*1.25u*PW),
(2*900n*PW+(floor(2/2)-1)*1.25u*PW))' PS='if(0, (2*900n+PW+PW*1+floor(2/
2)*2*(1.25u+PW*1)), (2*2*900n+PW+PW*1+(floor(2/2)-1)*2*(1.25u+PW*1)))'
AD='if(0, (900n*PW+floor(2/2)*1.25u*PW), floor(2/2)*1.25u*PW)' PD='if(0,
(2*900n+PW+PW*1+floor(2/2)*2*(1.25u+PW*1)), floor(2/2)*2*(1.25u+PW*1))'
MP2 Out B Vdd Vdd PMOS W=PW L=L M=2 AS='if(0,
(900n*PW+floor(2/2)*1.25u*PW),
(2*900n*PW+(floor(2/2)-1)*1.25u*PW))' PS='if(0, (2*900n+PW+PW*1+floor(2/
2)*2*(1.25u+PW*1)), (2*2*900n+PW+PW*1+(floor(2/2)-1)*2*(1.25u+PW*1)))'
AD='if(0, (900n*PW+floor(2/2)*1.25u*PW), floor(2/2)*1.25u*PW)' PD='if(0,
(2*900n+PW+PW*1+floor(2/2)*2*(1.25u+PW*1)), floor(2/2)*2*(1.25u+PW*1))'
MN1 Out A 1 0 NMOS W=NW L=L AS='if(1, (900n*NW+floor(1/2)*1.25u*NW),
(2*900n*NW+(floor(1/2)-1)*1.25u*NW))' PS='if(1, (2*900n+NW+NW*1+floor(1/
2)*2*(1.25u+NW*1)), (2*2*900n+NW+NW*1+(floor(1/2)-1)*2*(1.25u+NW*1)))'
AD='if(1, (900n*NW+floor(1/2)*1.25u*NW), floor(1/2)*1.25u*NW)' PD='if(1,
(2*900n+NW+NW*1+floor(1/2)*2*(1.25u+NW*1)), floor(1/2)*2*(1.25u+NW*1))'
```

```
MN2 1 B Gnd 0 NMOS W=NW L=L AS='if(1, (900n*NW+floor(1/2)*1.25u*NW),
(2*900n*NW+(floor(1/2)-1)*1.25u*NW))' PS='if(1, (2*900n+NW+NW*1+floor(1/
2)*2*(1.25u+NW*1)), (2*2*900n+NW+NW*1+(floor(1/2)-1)*2*(1.25u+NW*1)))'
AD='if(1, (900n*NW+floor(1/2)*1.25u*NW), floor(1/2)*1.25u*NW)' PD='if(1,
(2*900n+NW+NW*1+floor(1/2)*2*(1.25u+NW*1)), floor(1/2)*2*(1.25u+NW*1))'
.ends

*-------- Devices: SPICE.ORDER == 0 --------

VVin Vin Gnd PULSE(0 Vpwr 0 1n 1n 49n 100n)
XX1 Vin N_1 Out Gnd Vdd NAND L=500n NW=4u PW=8u
VVb N_1 Gnd DC 5
VVpower Vdd Gnd DC Vpwr

*-------- Devices: SPICE.ORDER > 0 --------

.PRINT TRAN V(Out)
.PRINT TRAN V(Vin)

.PRINT TRAN V(X1/1)

********* Simulation Settings - Analysis section *********

.tran 250p 300n

********* Simulation Settings - Additional SPICE commands *********

.end
```

Subcircuits are defined by blocks of device statements bracketed with the **.SUBCKT** and **.ENDS** commands, and *instanced* by statements beginning with the key letter **X**.

The **.SUBCKT** command includes the name of the subcircuit being defined (**NAND**), a list of terminals, and three subcircuit parameters. The *terminals* do not have a predefined order, but whatever order is used in the definition must be used in instances. *Parameters* can be written in any order in both the definition and the instances. If a parameter value is not specified in the instance the value in the definition is used as the default.

Within the subcircuit definition, four MOSFETs are defined in the usual manner—and in these statements the order of terminals *is* important: drain–gate–source–bulk. Node **1** is the source of transistor **MN1** and the drain of transistor **MN2**. Subcircuit parameters, enclosed by single quotes, are used in place of numerical values.

After the subcircuit is defined, you can create an instance of the subcircuit. The instance statement begins with the key letter **X**. The name of the instance, by which it is to be identified in the rest of the input file, is **X1** (not "XX1.")

The list of terminals in the instance statement must have the same order as on the first line of the subcircuit definition so that **A B Out Gnd** in the definition corresponds to **Vin N_1 OUT Gnd** in the instance. The next argument of the instance statement is the original subcircuit name **NAND**.

The default subcircuit parameter values, as specified by the definition, are overridden by instancespecific value assignments, which can appear in any order. Any parameters omitted from the instance statement retains its default value.

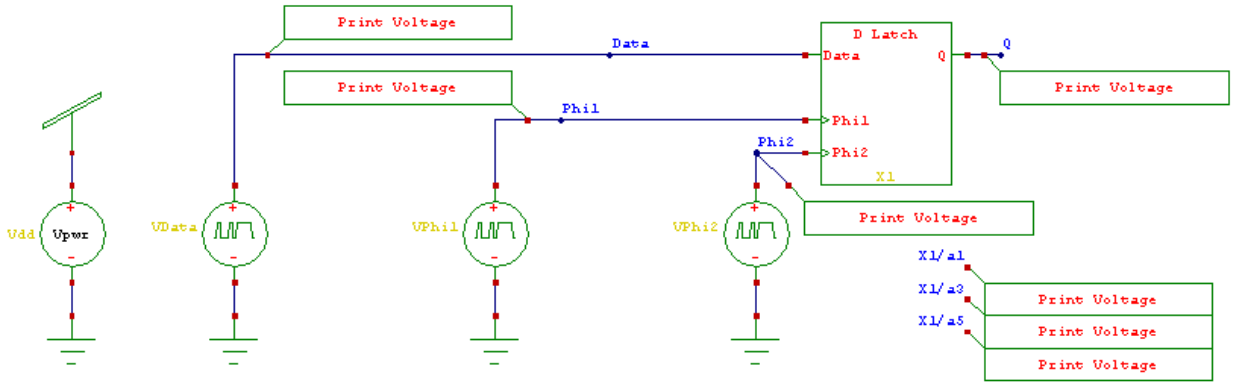
A standard DC operating point calculation (.OP) analysis is carried out on this circuit, with a duration of 300 nanoseconds and a maximum timestep of 250 picoseconds. The **.param** command sets the initial node voltages to 3.3 volts. The .PRINT command reports simulation results for the voltages at nodes
Vin, **OUT**, and **X1/N_1**.

Output

CHAPTER 7: TRANSIENT ANALYSIS—CMOS D-LATCH

Transient analysis on a CMOS static D-latch demonstrates the analog D-latch characteristics of a digital circuit. The circuit has four inverters and four transmission gates.

Schematic



T-Spice Input

********* Simulation Settings - Parameters and SPICE Options *********

.param Vpwr = 3.3v
.option NUMDGT = 2

*-------- Devices: SPICE.ORDER == 0 --------

VVdd Vdd Gnd DC Vpwr
VVData Data Gnd BIT({1000} PW=16n ON=Vpwr RT=500p FT=500p LT=15.5n HT=15.5n)
VVPhi1 Phi1 Gnd BIT({0011} PW=8n ON=Vpwr RT=500p FT=500p LT=7.5n HT=7.5n)
VVPhi2 Phi2 Gnd BIT({1100} PW=8n ON=Vpwr RT=500p FT=500p LT=7.5n HT=7.5n)
XX1 Q Data Phi1 Phi2 Gnd Vdd DLatch

*-------- Devices: SPICE.ORDER > 0 --------

.PRINT TRAN V(Q)

```
.PRINT TRAN V(X1/a1)
.PRINT TRAN V(X1/a3)
.PRINT TRAN V(X1/a5)
.PRINT TRAN V(Data)
.PRINT TRAN V(Phi1)
.PRINT TRAN V(Phi2)

********* Simulation Settings - Analysis section *********
.op

.tran 75ps 300ns

********* Simulation Settings - Additional SPICE commands *********

.end
```

Voltage source **VDD** sets the voltage between power and ground to the **Vpwr** parameter value of 3.3 volts.
The next three statements beginning with **V** define voltage sources for custom input waveforms. Following each voltage source name are the names of the input nodes (Data, Phi1, Phi2) and the type of waveform. Here, however, not piecewise linear but rather *bit* waveforms are used.

Following the keyword **BIT** in parentheses are parameters specifying the waveform characteristics. The four-digit sequence in braces **{ }** specifies the sequence of the wave's states (either **1**, "on," or **0**, "off"). This sequence will be repeated until the simulation is complete. The pulse widths (**PW**) are 16, 8 and 8 nanoseconds, respectively. The **OFF** voltage is zero, the **ON** voltage is 3.3 volts, the rise (**RT**) and fall (**FT**) times are each 500 picoseconds, and the low time (**LT**) and high time (**HT**) are both 7.5 nanoseconds.

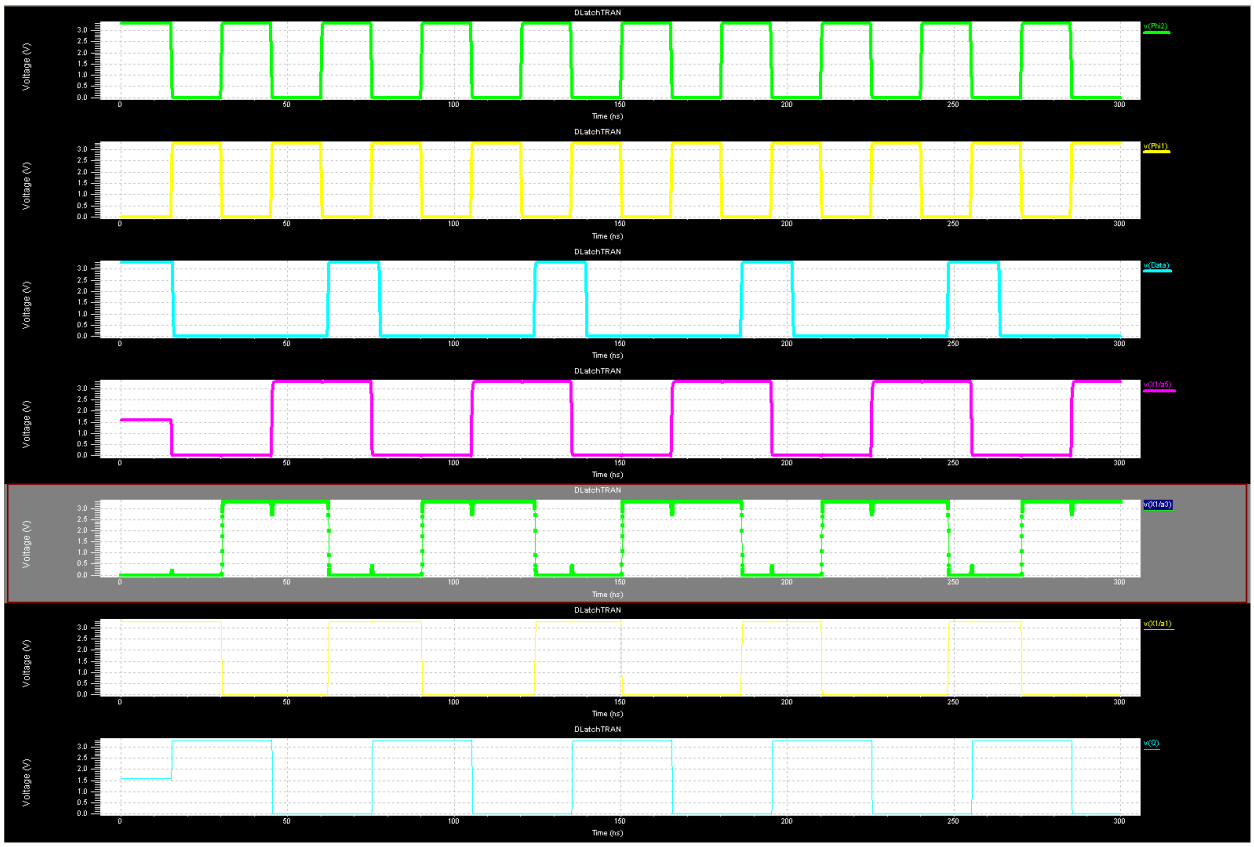
The **.TRAN** command instructs T-Spice to perform a 300-nanosecond simulation while printing node voltages at least every 75 picoseconds.

The **.PRINT** commands write simulation results for the voltages at each of seven nodes to the specified file.

Output

The following chart shows the seven output voltages measured during simulation, plotted across time. The chart is expanded and the traces are displayed in the same order in which they were loaded. Traces can be loaded or unloaded on a chart using *Chart > Options—Format* in W-Edit.

Note that when a trace is added to an existing chart, scaling of the axes is not automatically updated. To rescale the axes for optimal display, you can use the **HOME** key. Select *Chart > Options—Axes* to choose appropriate spacing of the major and minor tick marks.


DLatchTRAN
Voltage (V)
Time (ns)
v(Pin2)
DLatchTRAN
Voltage (V)
Time (ns)
v(Pin1)
DLatchTRAN
Voltage (V)
Time (ns)
v(Data)
DLatchTRAN
Voltage (V)
Time (ns)
v(X1/a5)
DLatchTRAN
Voltage (V)
Time (ns)
v(X1/a3)
DLatchTRAN
Voltage (V)
Time (ns)
v(X1/a1)
DLatchTRAN
Voltage (V)
Time (ns)
v(5)

CHAPTER 8: COMMAND REFERENCE

- **File Menu**

Command	*Shortcut*
File > New > Design	
File > New > File	**Ctrl+N**
File > Open > Open Design	**Ctrl+O**
File > Open > **Add Library** **Open File** **Execute Script**	
File > Save > Save Design	**Ctrl+S**
File > Save > **Save Design and Its Libraries** **Save Selected Design/Libraries** **Save copy of Selected Design/Libraries**	
File > Close > **{*Design* }** **Remove Library** **Close File**	
File > Import > **Import EDIF** **Import Spice**	
File > Export > **Export EDIF** **Export Spice** **Export Verilog** **Export VHDL** **Export TPR**	
File > Page Setup	
File > Print Preview	
File > Print	**Ctrl+P**
File > Recent Files	

File > Recent Scripts

File > Exit

- **Edit Menu**

Command	*Shortcut*
Edit > Undo	**Ctrl+Z, Alt+Back**
Edit > Redo	**Ctrl+Y**
Edit > Cut	**Ctrl+X**
Edit > Copy	**Ctrl+C**
Edit > Paste	**Ctrl+V**
Edit > Clear Del	
Edit > Duplicate	**Ctrl+D**
Edit > Capture Window	
Edit > Select All	**Ctrl+A**
Edit > Deselect All	**Alt+A**
Edit > Find	
Edit > Edit-in-Place > Push Into Page Down	
Edit > Edit-in-Place > Pop Out Page Up	

- **View Menu**

Command	*Shortcut*
View > Fit Home	
View > Exchange	**X**
View > Goto > Goto Previous	
View > Goto > Goto Next	
View > Goto > Goto Coordinates	
View > Zoom > Mouse Zoom	**Z**
View > Zoom > Zoom In	**+**
View > Zoom > Zoom Out	**-**

View > Zoom > Zoom to Selections **W**

View > Zoom > Pan to Selections

Command	*Shortcut*

View > Pan > Pan Left

View > Pan > Pan Right

View > Pan > Pan Up

View > Pan > Pan Down

View > Pan > Edge

View > Library Navigator

View > Properties

View > View Navigator

View > Status Bar

View > Command Window

View > Activate Command Window **‘**

View > Toolbars >
- **Standard**
- **Draw**
- **Segment**
- **Electrical**
- **SPICE Simulation**
- **Locator**
- **Mouse Buttons**

View > Cell View > Cycle View **?**

View > Objects >
- **Visible**
- **Selectable**

View > Display >
- **Display Major Grid**
- **Display Minor Grid**
- **Display Origin**
- **Display Evaluated Properties**

View > Redraw Space

- **Draw Menu**

Command	*Shortcut*
Draw > Move By	
Draw > Force Move	Alt + M
Draw > Rotate	R
Draw > Flip > Flip Horizontal	H
Draw > Flip > Flip Vertical	V
Draw > Select	
Draw > Box	B
Draw > Polygon	P
Draw > Path	
Draw > Circle	
Draw > Text Label	
Draw > Electrical >	
Wire	
Solder Point	
Connect/Disconnect	
Net Cap	
Net Label	
In Port	
Out Port	
In/Out Port	
Other Port	
Global Port	
Property	

- **Cell Menu**

Command	*Shortcut*
Cell > New View	N
Cell > Open View	O
Cell > Copy View	
Cell > Rename View	
Cell > Delete View	

Cell > Page

New Page

Delete Page

Command	*Shortcut*

Rename Page

Previous Page

Next Page

Open Page

Cell > Copy Cell

Cell > Rename Cell

Cell > Redirect Instances

Cell > Generate Symbol

Cell > Instance I

- **Setup Menu**

Command	*Shortcut*
Setup > Technology	
Page > Preferences	
Page > SPICE Simulation	

- **Tools Menu**

Command	*Shortcut*
Tools > Design Checks	
Tools > Highlight Net	
Tools > Start Simulation	
Tools > T-Spice	
Tools > Probe	**V**
Tools > Probe	**I**
Tools > Probe	**Q**
Tools > User > (User 1...10)	

- **Window Menu**

Command	*Shortcut*
Window > Dockable	
Window > Auto Hide	
Window > Hide	

Window > Floating
Window > Close

Window > Cascade

Window > New Window

Window > Tile

Window > Arrange Icons

Window > Close All Except Active

Window > Theme

Window > (recently opened files)

- **Help Menu**

Command ***Shortcut***

Help > Schematic Editor Manual

Help > Release Notes

Help > Tutorial

Help > S-Edit Examples Guide

Help > Setup Examples and Tutorial

Help > Commuter Licenses

Help > Support

Help > About S-Edit

CHAPTER 9: EXPERIMENTS USING T-SPICE

In this chapter some experiments related with university syllabus are described. These experiments will describe how to write a laboratory copy and how experiments will be performed.

The three experiments are described as they belong to syllabus. These are

1. Experiment No. 1: To design and implementation of a two input NAND gate using TSPICE.
2. Experiment No. 2: To design and implementation of a two input NOR gate using TSPICE.
3. Experiment No. 3: To design and implementation of a two input XOR gate using TSPICE.

EXPERIMENT NUMBER: - Date:-

DESIGN & IMPLEMENTATION OF CMOS NAND GATE USING T-SPICE

OBJECTIVE:-

To design and implementation of a two input NAND gate using TSPICE and analyze the Transient characteristics of output waveform.

THEORY:

If we take Va as 1st input of the NAND gate, & Vb as 2nd input of the NAND gate then output can be expressed as-

Vout = (Va.Vb)'.

Which may also be expressed as- Vout = (Va.Vb)' = Va'+Vb'.

It must be noted as the output of this circuit is just the opposite of AND gate (initially observed).

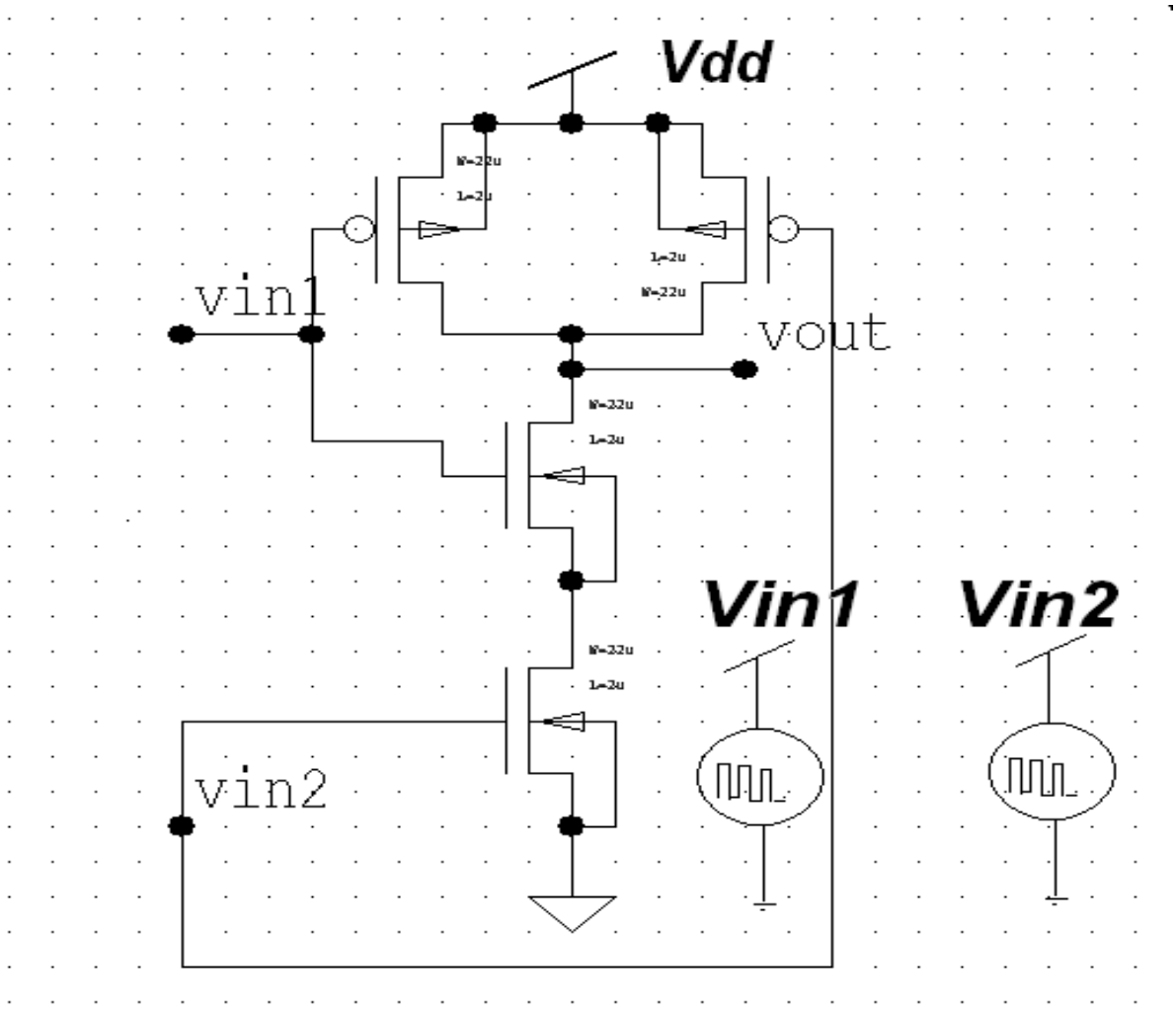
TRUTH TABLE:

Va	Vb	Va.Vb	(Va.Vb)'
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

BOOLEAN EXPRESSION:

Vout = (Va.Vb)' = Va' + Vb'.

SCHEMATIC DIAGRAM OF THE CIRCUIT:



CIRCUIT DESCRIPTION:

In this experiment, we have used CMOS logic design technique.
Here f = (Va.Vb)'=Va' +Vb'
So, f' = ((Va.Vb)')'=Va.Vb
Now use f for pMOS circuit design & use f' for nMOS circuit design. Where boolean (.) indicate series operation and Boolean (+) signifies parallel operation.Based on this, we built the given circuit and simulate using TSPICE to observe the output waveform.
As per the above methodology two pMOS connected in parallel and two nMOS connected in series. Collecting output from their common node mentioned as Vout.

We gave two common inputs (Va and Vb) to both the circuit parts.

NETLIST:

```
* SPICE netlist written by S-Edit Win32 Demo 9.12
* Written on Apr 2, 2009 at 10:45:05

* Waveform probing commands

.probe
.options probefilename="NAND_GATE.dat"
+ probesdbfile="G:\ NAND_GATE.sdb"
+ probetopmodule=" NAND_GATE”

* Main circuit: NAND_GATE

M1 vout vin1 N2 N2 NMOS L=2u W=44u AD=66p PD=24u AS=66p PS=24u
 M2 N2 vin2 Gnd Gnd NMOS L=2u W=44u AD=66p PD=24u AS=66p PS=24u
 M3 vout vin1 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M4 Vdd vin2 vout Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
v5 vin1 Gnd bit ({0100} pw=100n on=5.0 off=0.0 rt=1n ft=1n delay=0 lt=100n ht=100n)
v6 vin2 Gnd bit ({1111} pw=100n on=5.0 off=0.0 rt=1n ft=1n delay=0 lt=100n ht=100n)

.include "C:\Program Files\Tanner EDA\Demo\T-Spice\models\ml2_125.md"
vdd vdd gnd 5

.tran 1n 400n
.print tran v(vin1) v(vin2) v(vout)
```

OUTPUT WAVEFORM:

CONCLUSION:

After performing the above experiment we come to know about the operation of a NAND gate using T-SPICE .here we have performed the operation of a 2 input NAND gate which is basically a multiplication operation between two inputs. We have done dc & transient operation of the NAND gate. In the dc operation there is lots of noise interference in the output waveform which are eliminated in the transient operation by using source voltage bit instead of a dc input. As a result we got an output waveform as shown above.

EXPERIMENT NUMBER: - Date:-

DESIGN & IMPLEMENTATION OF CMOS NOR GATE USING T-SPICE

OBJECTIVE:-

To design and implementation of a two input NOR gate using TSPICE and analyze the Transient characteristics of output waveform.

THEORY:

If we take Va as 1st input of the NOR gate, & Vb as 2nd input of the NOR gate then output can be expressed as-

Vout = (Va+Vb)'.

Which may also be expressed as- Vout = (Va+Vb)' = Va'.Vb'.

It must be noted as the output of this circuit is just the opposite of OR gate (initially observed).

Truth table:

Input = A	Input = B	Output = Y
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**

BOOLEAN EXPRESSION :

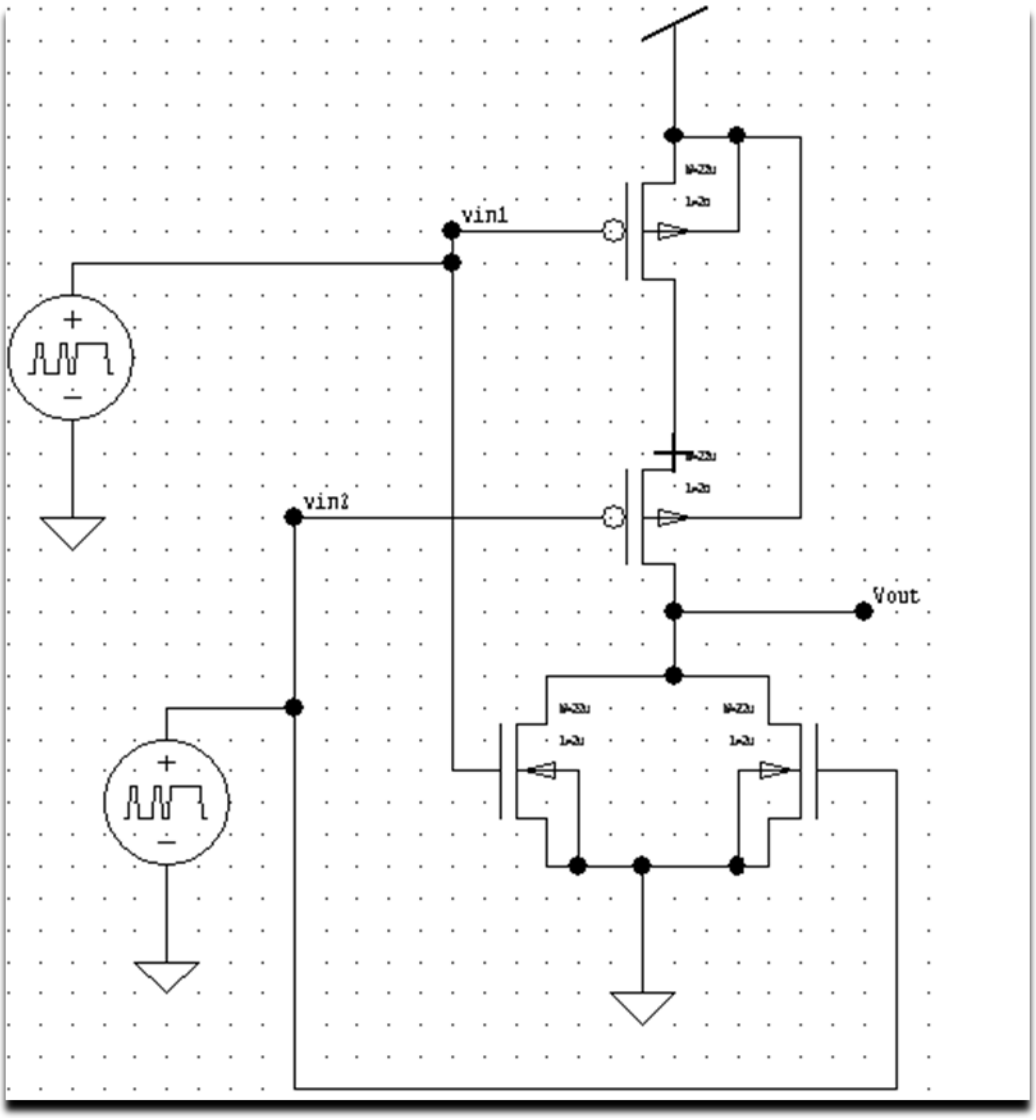
The Boolean Expression of the circuit is :

F = (A+B) ' = (A'.B').

F’ = ((A+B)’)’= A+B.

CIRCUIT DIAGRAM:

The circuit diagram for the same is shown as



CIRCUIT ANALYSIS:

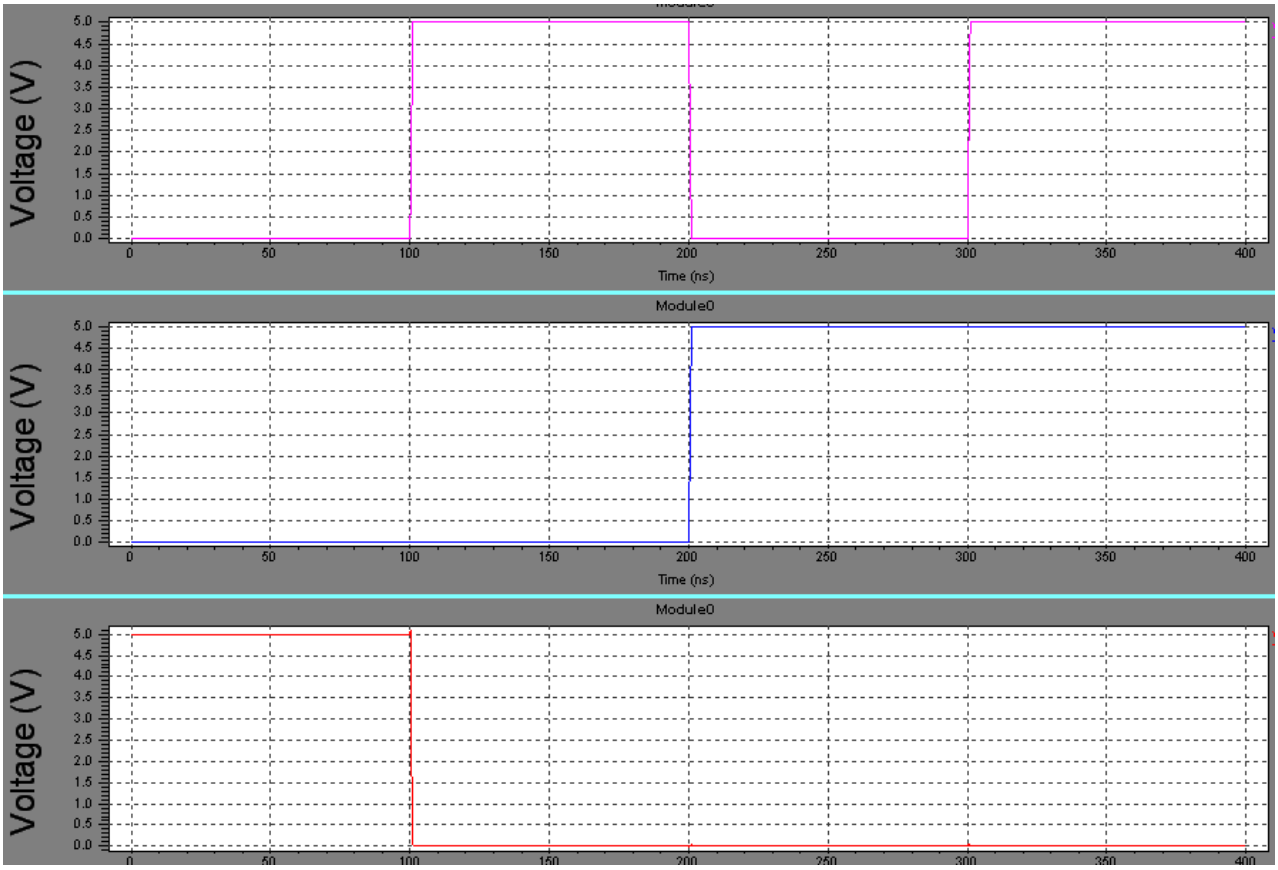
The above circuit consists of two PMOS in series and two NMOS in parallel. When both the input is low we get the Vdd as the Vout. But when any of the or both the input is high then the route for the current is blocked by one or both of the PMOS. But at that time the current finds

alternate path from the ground as one or both of the NMOS is ON and they are in parallel. Hence we get output as low.

NETLIST:

```
* Written on Mar 26, 2009 at 09:58:50

* Waveform probing commands

.probe

.options probefilename="NOR1.dat"

+ probesdbfile="D:\NOR1.sdb"

+ probetopmodule="NOR"


* Main circuit: NOR

M1 Vout vin2 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

M2 Vout vin1 Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

M3 N3 vin1 Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

M4 Vout vin2 N3 Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u

v5 vin2 Gnd bit({10011} pw=100n on=5.0 off=0.0 rt=10n ft=10n delay=0 lt=10n ht=10n)

v6 vin1 Gnd bit({10011} pw=100n on=5.0 off=0.0 rt=10n ft=10n delay=0 lt=10n ht=10n)

.include "C:\Program Files\Tanner EDA\Demo\T-Spice\models\ml2_20.md"

vdd vdd gnd 5

.tran 1n 400n

.print v(vin1) v(vin2) v(vout)
```

OUTPUT WAVEFORM:



CONCLUSION:

The analysis of NOR gate using CMOS is done in T-SPICE. The circuit is combination of NMOS and PMOS. Output was high when both the input is Low. The output came as Low when one or both of the input was high. The graph is obtained from the circuit gives the characteristics of the NOR gate. But there is some delay due to the presence of rise time and fall time.

EXPERIMENT NUMBER:- Date:-

DESIGN & IMPLEMENTATION OF XOR GATE USING T-SPICE

OBJECTIVE:-

To design and implementation of a two input XOR gate using TSPICE and analyze the Transient characteristics of output waveform.

THEORY:

If we take Va as 1st input of the NAND gate, & Vb as 2nd input of the XOR gate then output can be expressed as-

Vout = (Va.Vb'+Vb.Va');

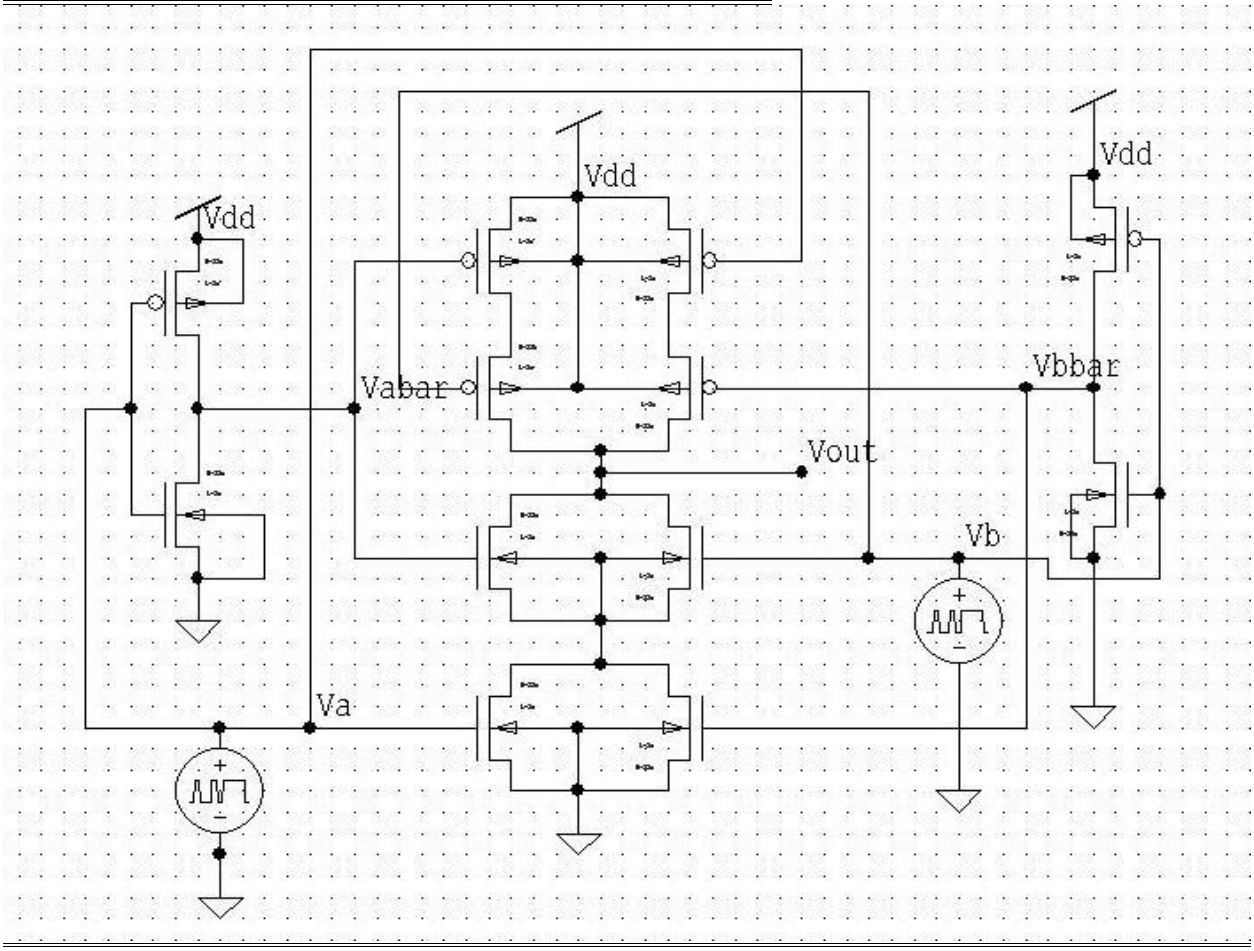
Truth table:

Input = A	Input = B	Output = Y
0	0	0
0	1	1
1	0	1
1	1	0

Boolean Expression:

Vout = (Va.Vb' + Vb.Va')

SCHEMATIC DIAGRAM OF THE CIRCUIT:



CIRCUIT DESCRIPTION:

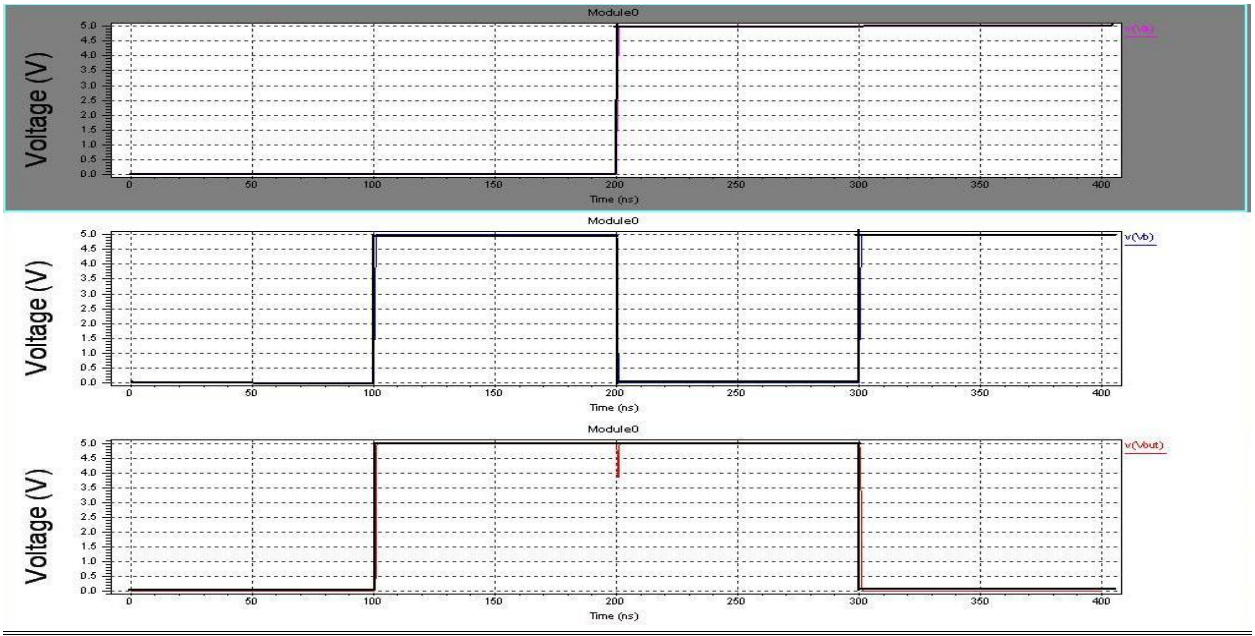
In this experiment, we have used CMOS logic design technique.
Here f = (Va.Vb'+ Vb.Va')
So, f' = (Va.Vb'+ Vb.Va')' = (Va+Vb') * (Va'+Vb);
Now use f for pMOS circuit design & use f' for nMOS circuit design. Where boolean (.) indicate series operation and Boolean (+) signifies parallel operation.Based on this, we built the given circuit and simulate using TSPICE to observe the output waveform.
As per the above methodology two pMOS connected in parallel and two nMOS connected in series. Collecting output from their common node mentioned as Vout.

NETLIST:

* Waveform probing commands
.probe

```
.options probefilename=" XOR.dat"
+ probesdbfile="D:\XOR.sdb"
+ probetopmodule="XOR"

* Main circuit: Anirban_XOR
.include "C:\Program Files\Tanner EDA\Demo\T-Spice\models\ml2_typ.md"
M1 N4 Vb Vout N4 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M2 Vout Vabar N4 N4 NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M3 N4 Va Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M4 Gnd Vbbar N4 Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M5 Vabar Va Gnd Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M6 Gnd Vb Vbbar Gnd NMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M7 N3 Vabar Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M8 Vdd Va N1 Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M9 Vout Vb N3 Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M10 N1 Vbbar Vout Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M11 Vabar Va Vdd Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M12 Vdd Vb Vbbar Vdd PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
v13 Va Gnd bit({0011} pw=100n on=5.0 off=0.0 rt=0n ft=0n delay=0 lt=100n ht=100n)
v14 Vb Gnd bit({0101} pw=100n on=5.0 off=0.0 rt=0n ft=0n delay=0 lt=100n ht=100n)
Vdd Vdd gnd 5v
.tran 1n 400n
.print tran V(Va) V(Vb) V(Vout)
```

OUTPUT WAVEFORM:



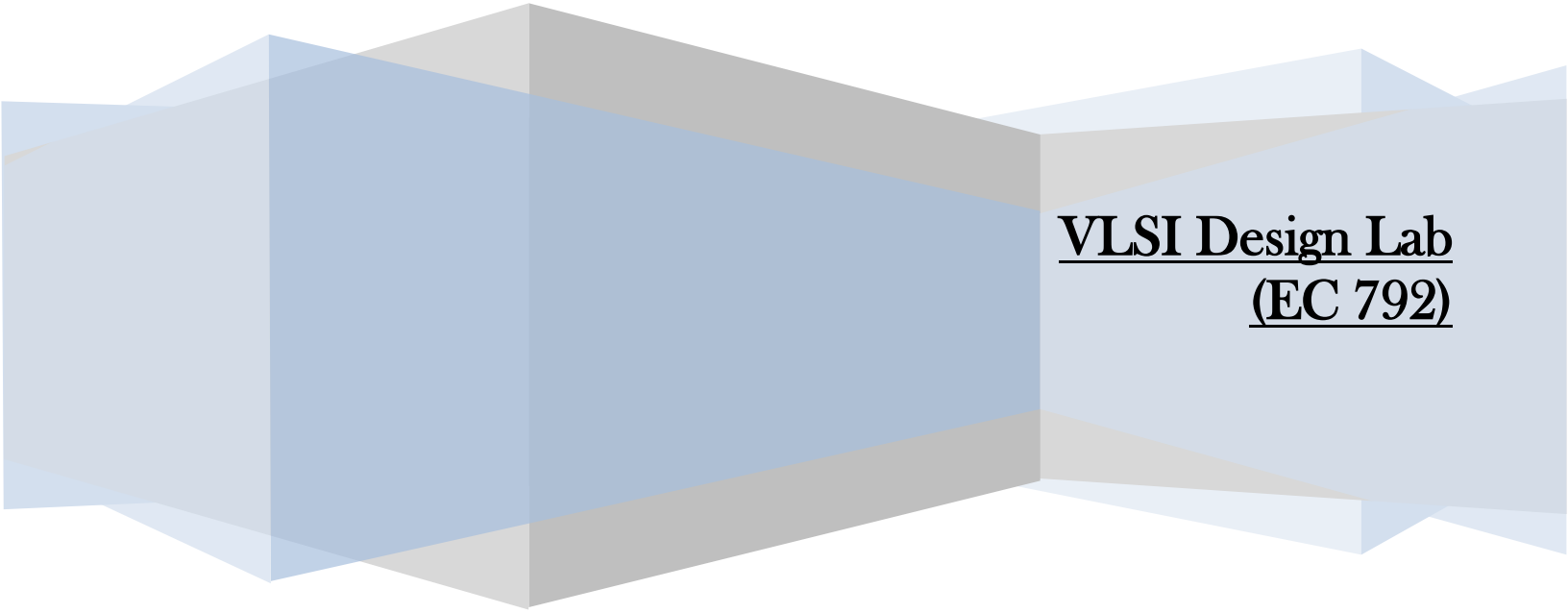
CONCLUSION:

After performing the above experiment we come to know about the operation of a XOR gate using T-SPICE. Here we have performed the operation of a 2 input XOR gate which is basically a multiplication operation between two inputs. We have done dc & transient operation of the XOR gate. In the dc operation there is lots of noise interference in the output waveform which are eliminated in the transient operation by using source voltage bit instead of a dc input. As a result we got a output waveform as shown above.

Laboratory Manual

PART- 2

FAMILIARITY WITH EDA TOOLS FOR VLSI DESIGN



VLSI Design Lab
(EC 792)

CHAPTER 10: SOFTWARE FAMILIARIZATION

Study of Simulation Tools

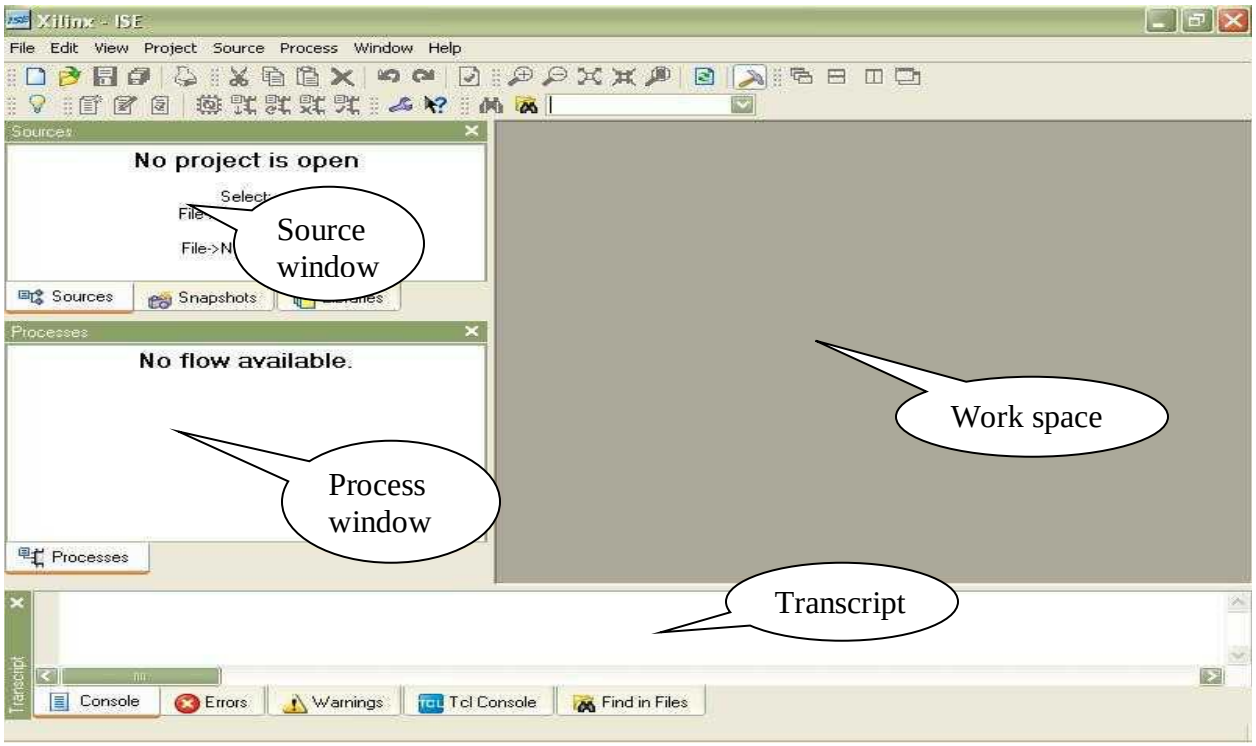
Simulation is functional emulation of the circuit design through software programs that uses models to replicate how a system will perform in terms of timings and results.

Xilinx ISE tool supports the following simulation tools:

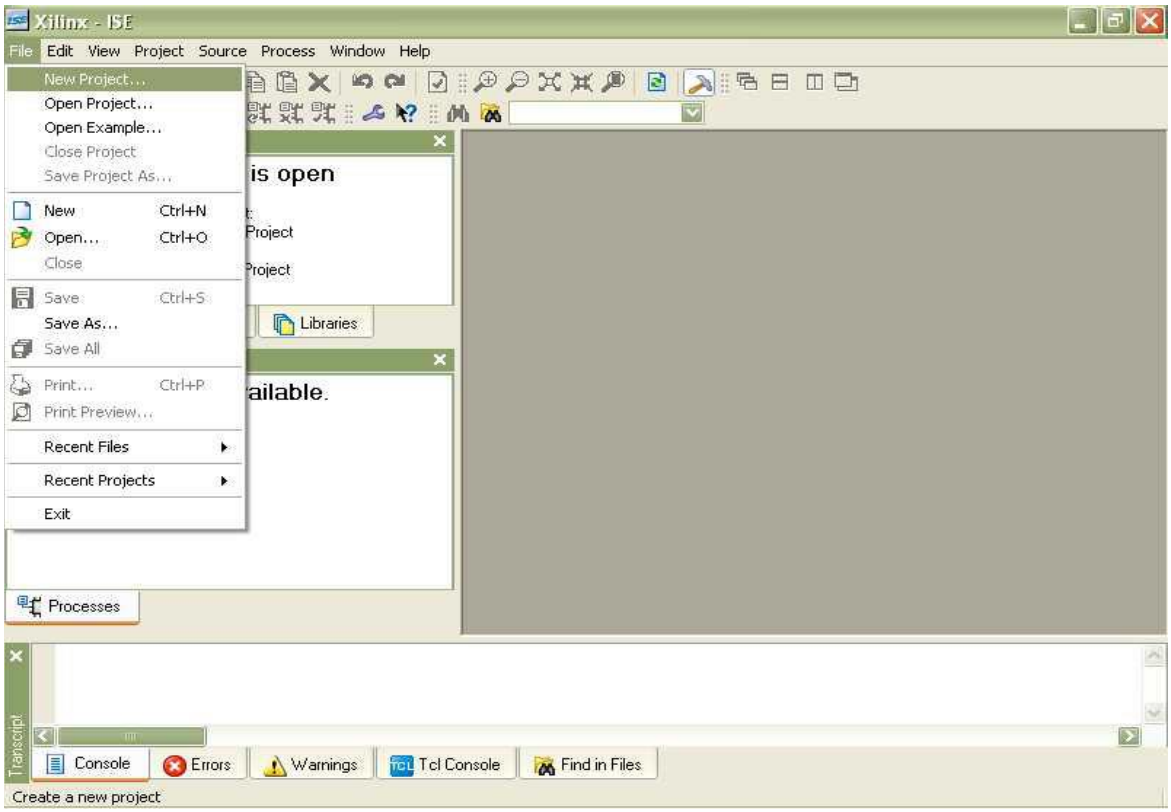
•HDL Bencher is an automated test bench creation tool. It is fully integrated with Project Navigator.

Simulation using Xilinx HDL Bencher:

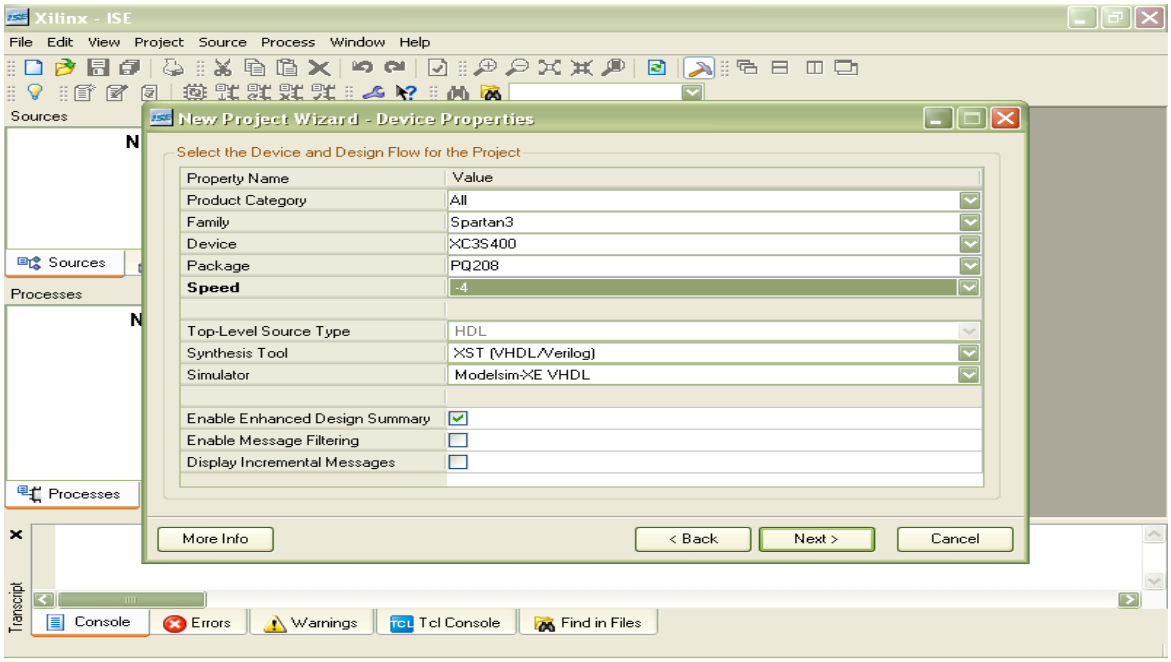
1. Start the Xilinx Project Navigator by using the desktop shortcut or by using the Start → Programs → Xilinx ISE.

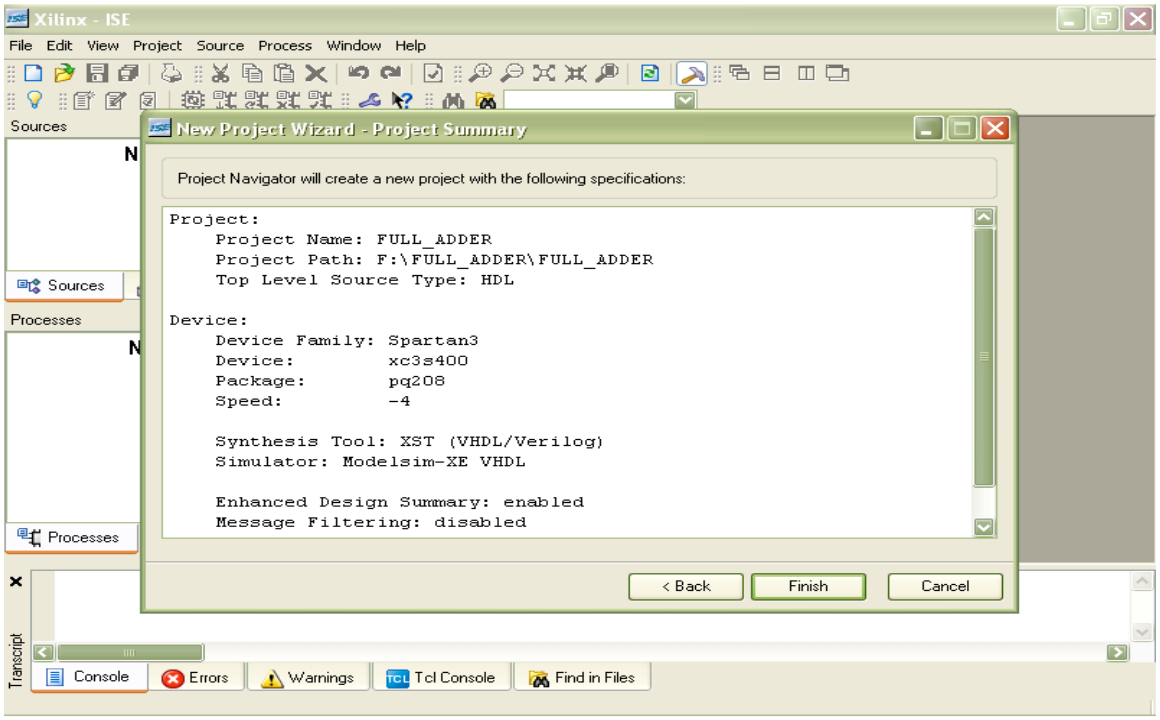


2. Create a new project.
   Select File menu and then select New project.



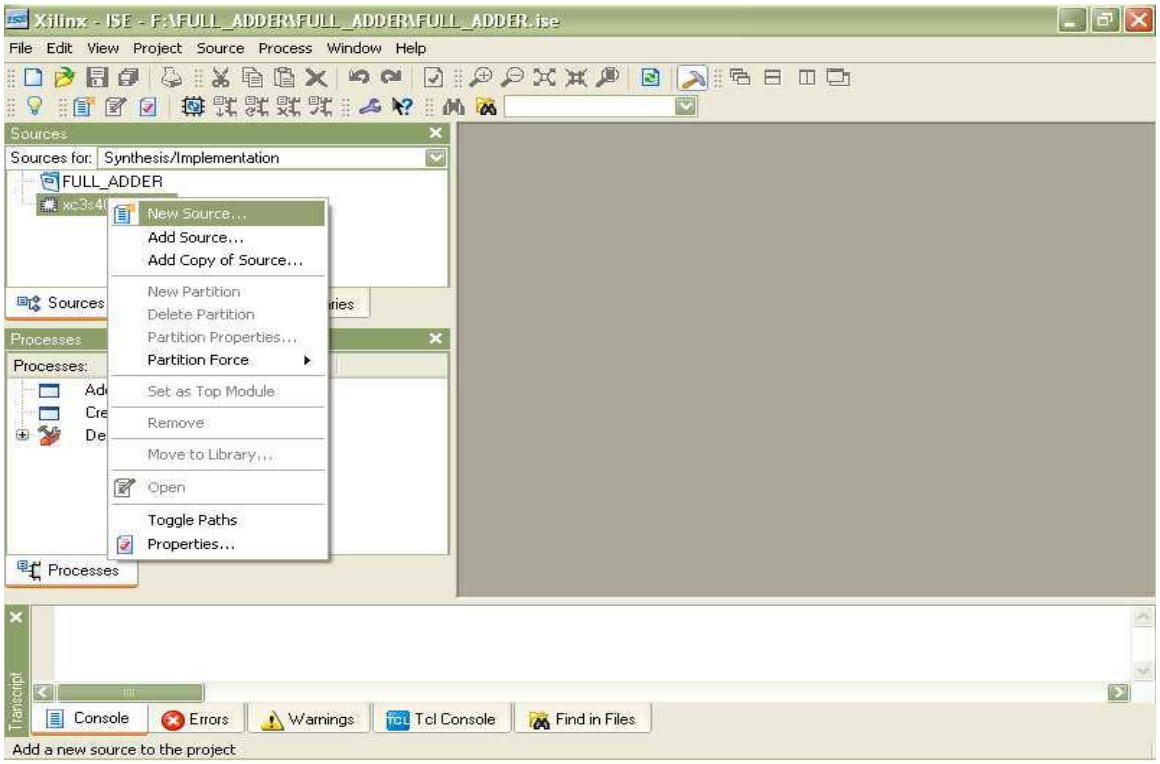
Specify the project name and location in pop up window and click NEXT.
Select Device. Select the required family, device, package, speed grade, Synthesis tool Simulator from new project wizard pop up window.
Click NEXT. Project summary will be displayed.



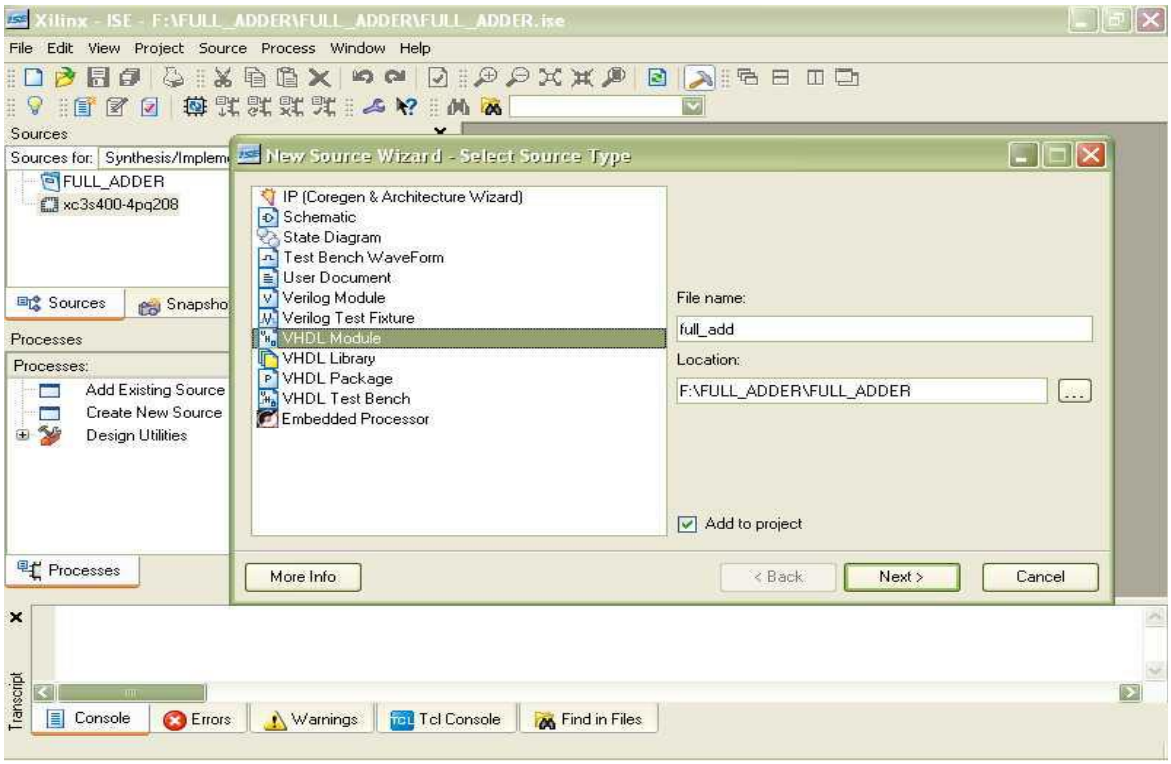


Click FINISH to start Project.

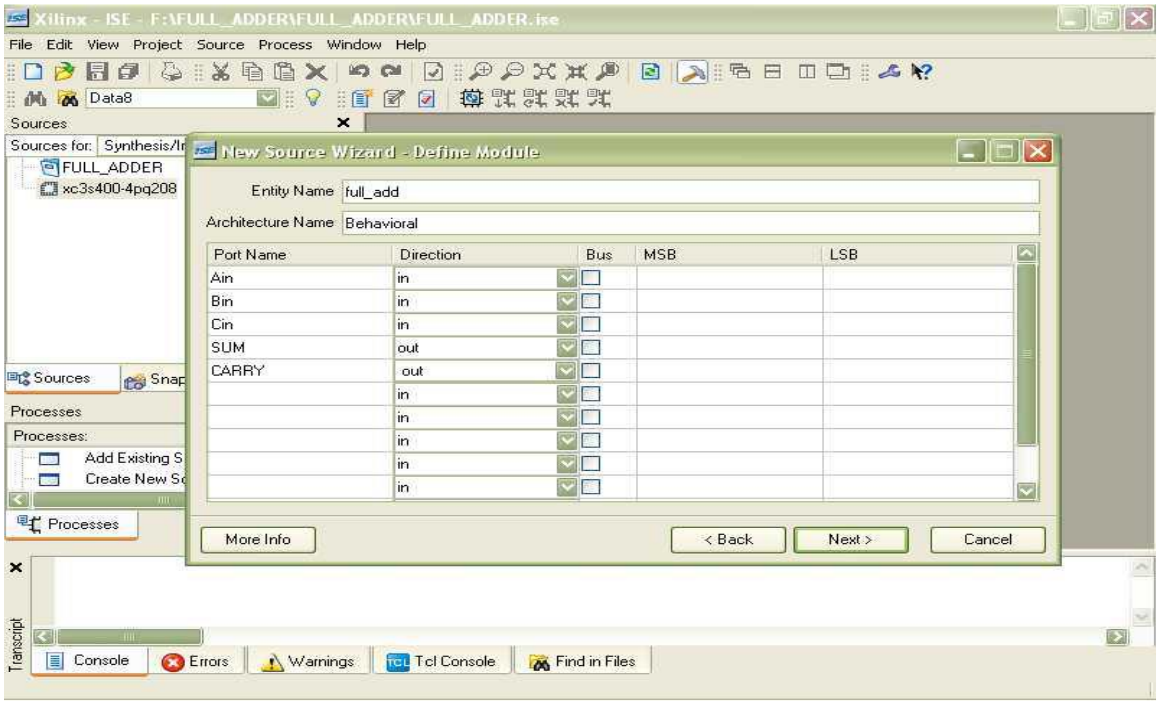
3. To create new VHD file Right click on the device name and select NEW SOURCE.



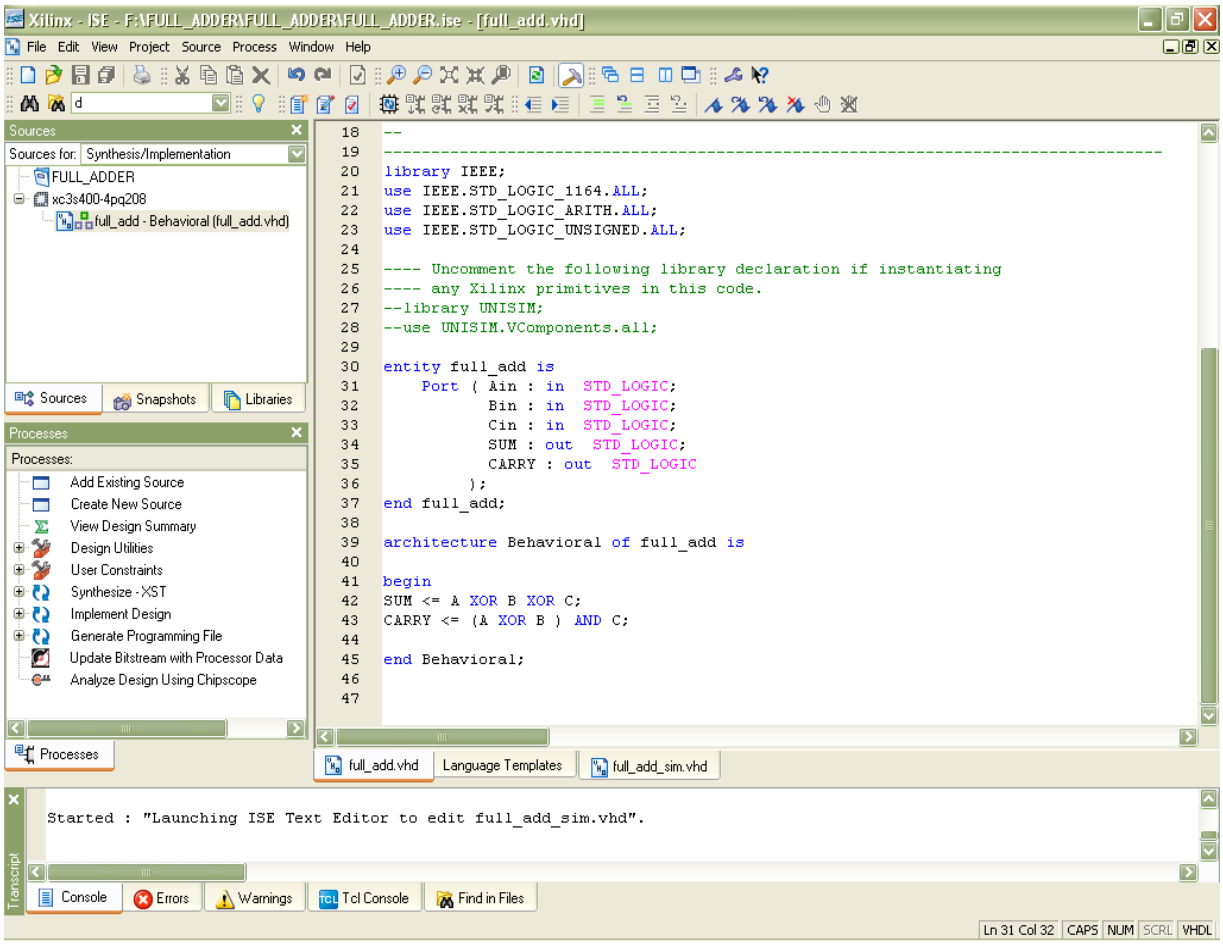
Select VHDL MODULE in NEW SOURCE WIZARD and give suitable name for theProject. Click NEXT for the DEFINE MODULE Window.



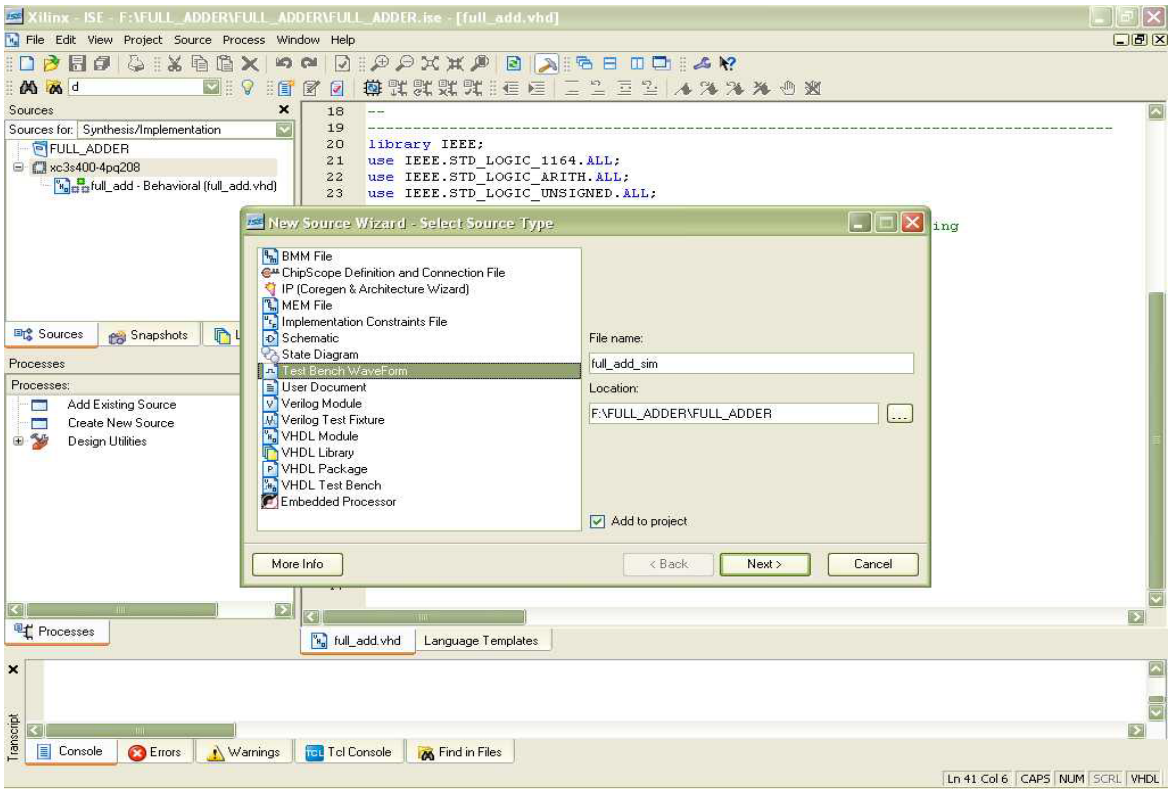
Assign required ports in this Window. The direction



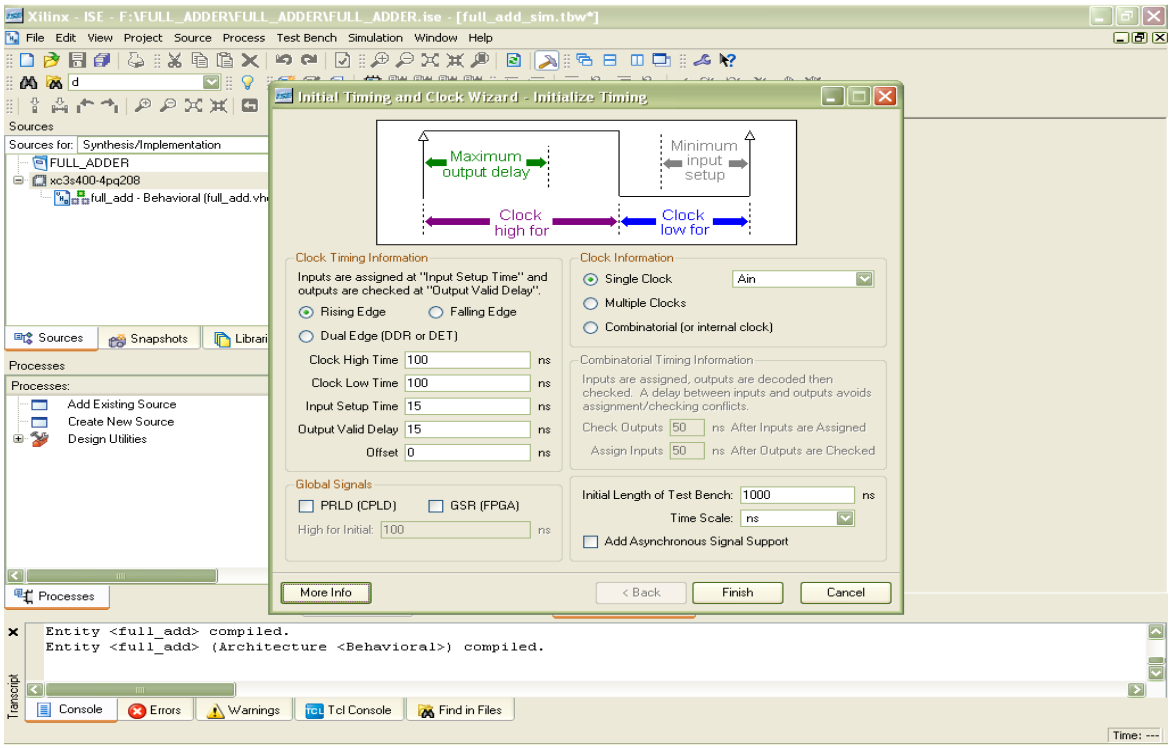
4. Write the Behavioural VHDL Code in VHDL Editor
   Sample code is given below for this experiment.



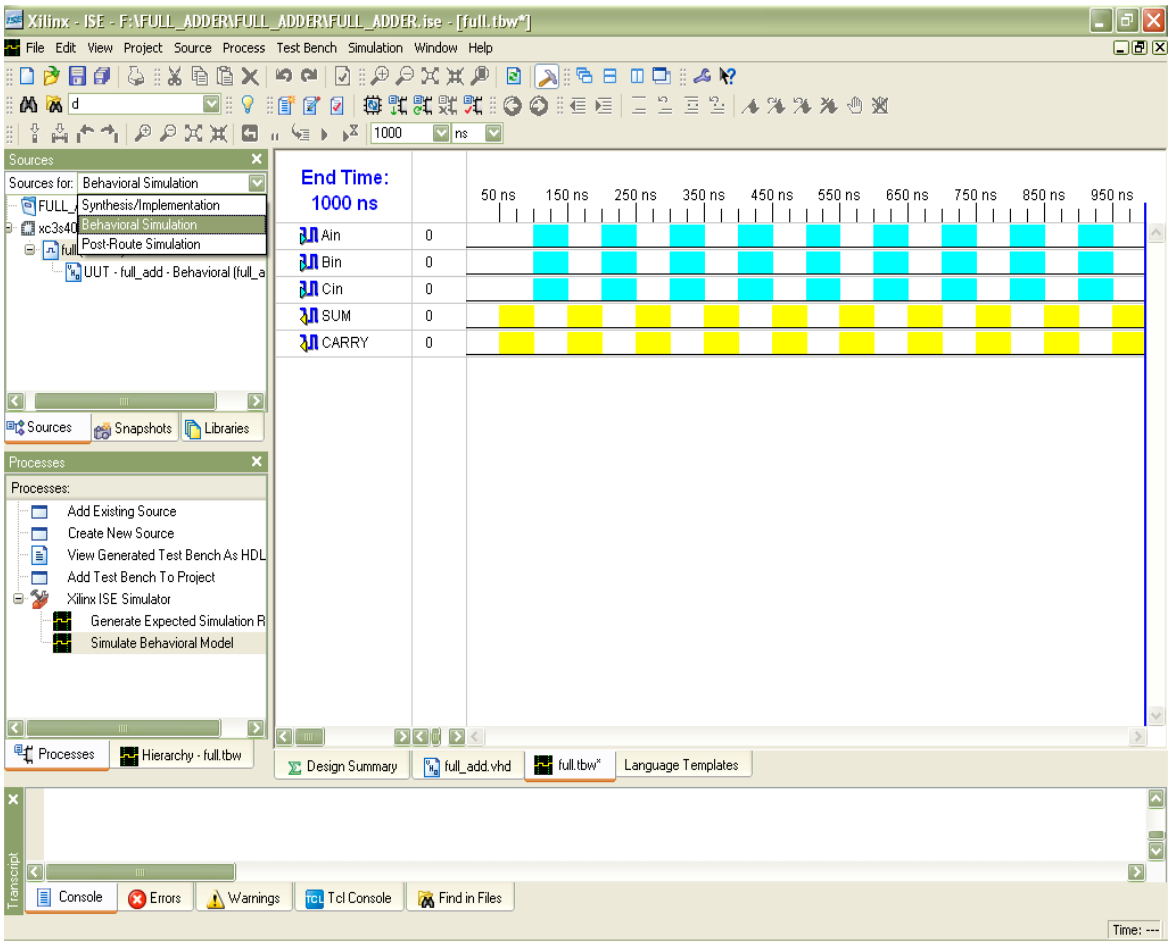
5. SIMULATION using ISE tool
   Creating a test bench file
   Verify the operation of your design before you implement it as hardware. Simulation can be done using ISE simulator. For this click on the symbol of FPGA device and then right click ⟶ Click on new source ⟶Test Bench Waveform and give the name ⟶ Select entity ⟶Finish.



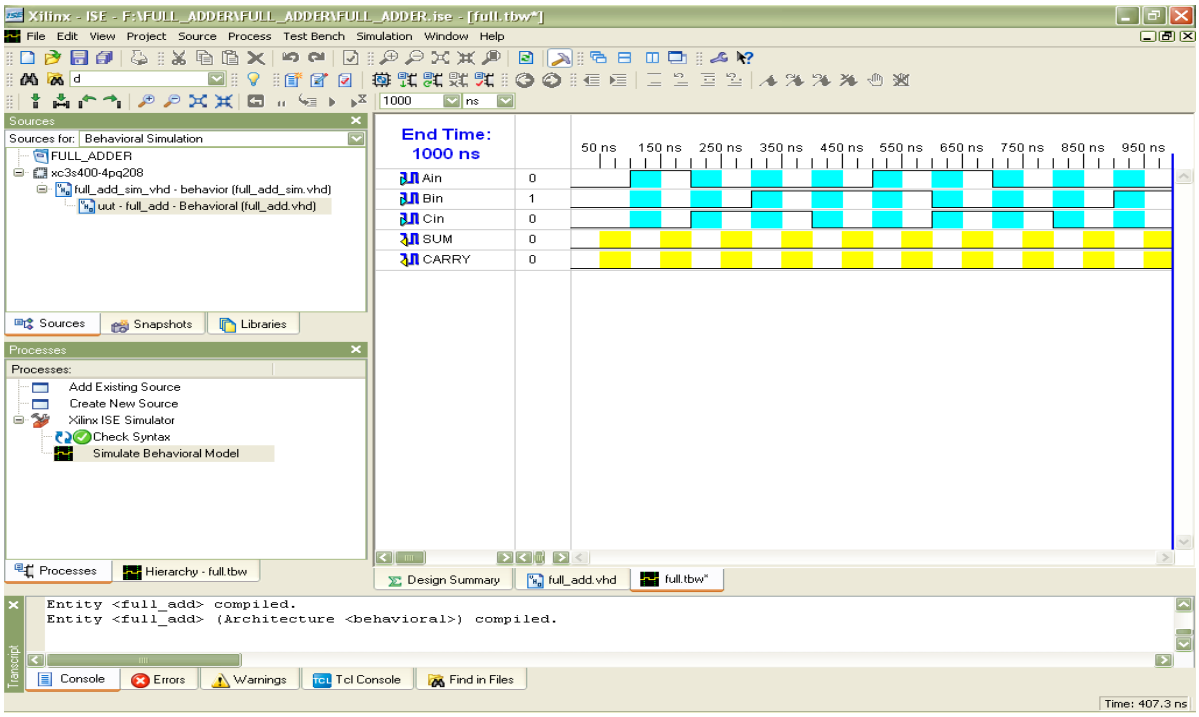
The window to Select Clock, Duty Cycle will appear. Select required parameters and say FINISH



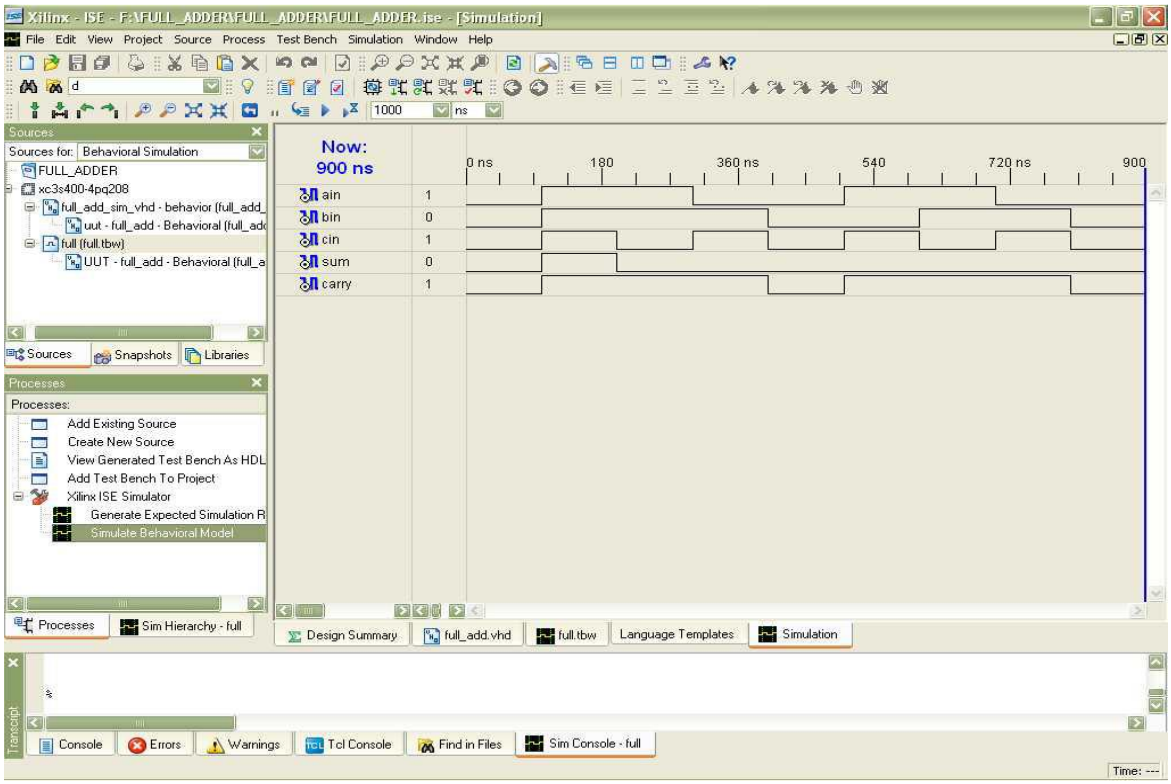
6. BEHAVIOURAL SIMULATION
   Select Behavioral Simulation from the scroll down list.



7. Give wave pattern on the input signals as required. Then double click on Simulate Behavioral Model for simulating.



The wave form according to the inputs given will appear in the window. The wave formcan be analyzed for the correctness of functionality.



CHAPTER 11: EXPERIMENTS USING Xilinx Software

In this chapter some experiments related with university syllabus are described. These experiments will describe how to write a laboratory copy and how experiments will be performed.

The three experiments are described as they belong to syllabus. These are

1. Experiment No. 5: Design & Implementation of CMOS Full adder Circuit using VHDL
2. Experiment No. 6: Design of CMOS D Flip flop using VHDL
3. Experiment No. 7: Design of n bit synchronous Counter using VHDL
4. Experiment No. 8: Design of shift register using VHDL.

EXPERIMENT NUMBER:- Date:-

DESIGN & IMPLEMENTATION OF FULL ADDER CIRCUIT USING VHDL

OBJECTIVE:-

Design and implementation of a Full Adder using VHDL with the help of Xilinx ISE.

THEORY:-

Full adder is the arithmetic circuit which adds two single bit input considering carry and produces sum bit and carry bit. Sum is obtained by **XOR** operation of the two inputs and the input carry. Considering the inputs as input1 & input2 and input carry as c_{in} of Full Adder Circuit, and then sum can be expressed as-

sum = input1 *XOR* input2 *XOR* c_{in}
= input1$\oplus$ input2 $\oplus$ c_{in};

And the output carry can be expressed as-

carry = input1 *AND* input2 *OR* input1 *AND* c_{in} *OR* input2 *AND* c_{in}
= input1.input2 + input1.c_{in} + input2.c_{in};

Truth table:

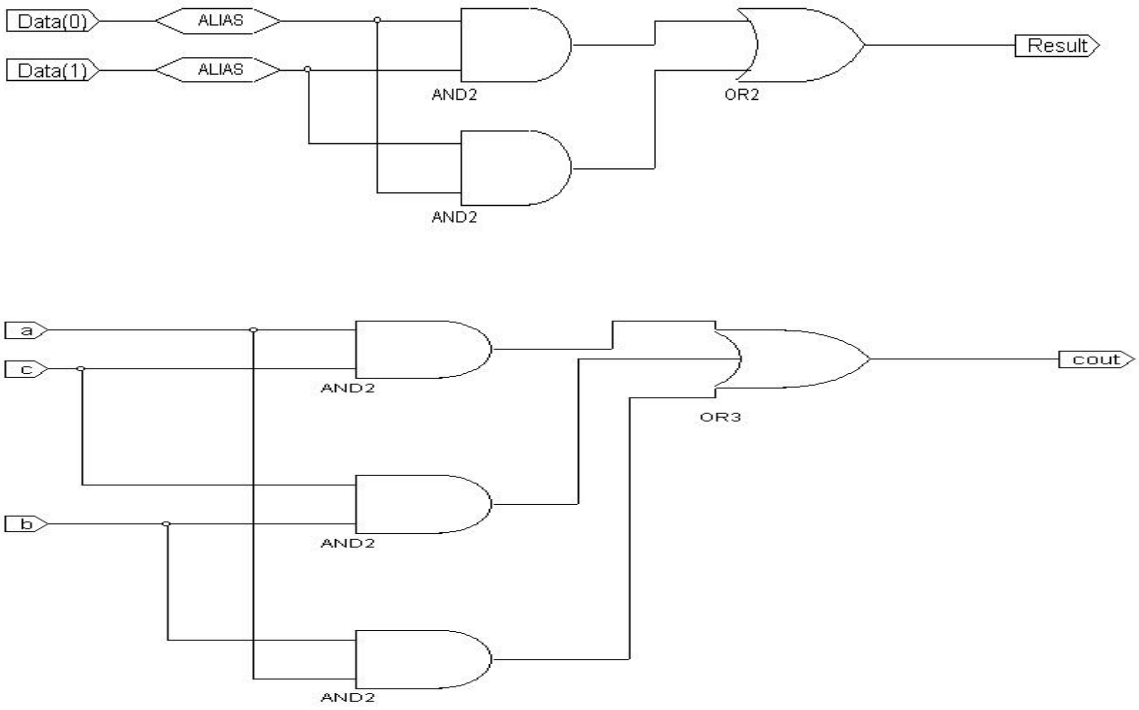
C_{in}=c	Input1=a	Input2=b	Sum	Carry=cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Expression:-

sum = input1 ***XOR*** input2 ***XOR*** c_{in}
= input1 $\oplus$ input2 $\oplus$ c_{in};

carry = input1 ***AND*** input2 ***OR*** input1 ***AND*** c_{in} ***OR*** input2 ***AND*** c_{in}
= input1.input2 + input1.c_{in} + input2.c_{in};

SCHEMATIC DIAGRAM OF THE CIRCUIT:-

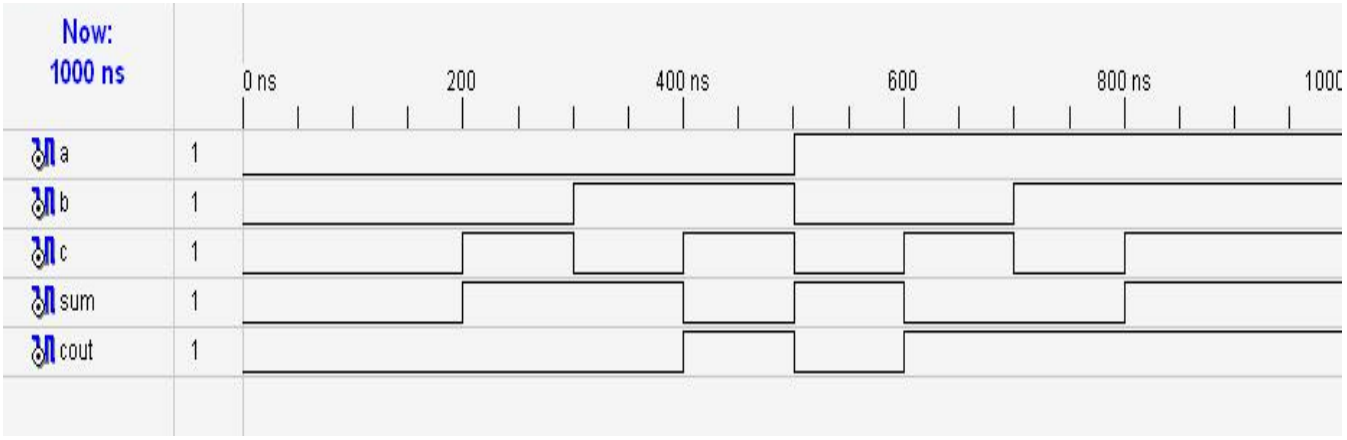


VHDL PROGRAM:-

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity fulladder is
Port ( a : in std_logic;
b : in std_logic;
c : in std_logic;
```

```
sum : out std_logic;
cout : out std_logic);
end fulladder;

architecture Behavioral of fulladder is
signal s:std_logic_vector(5 downto 0);
begin
s(0)<=a xor b;
s(1)<=s(0)xor c;
s(2)<=a and b;
s(3)<=b and c;
s(4)<=c and a;
s(5)<=s(2) or s(3) or s(4);
sum<=s(1):
cout<=s(5);
end Behavioral;
```

OUTPUT WAVEFORM:-



CONCLUSION:-

Full adder is the logic circuit which adds two logic input considering an input carry. The sum is as same as XOR of three inputs. And the output carry is AND of two inputs at time and OR of those. We have used VHDL language. Here we have used Behavioral modeling to build the program in Xilinx ISE.

EXPERIMENT NUMBER: - Date:-

REALIZATION OF D FLIPS FLOP USING XILINX SOFTWARE.

OBJECTIVE:-

Study & Realization of D flip flop.

THEORY:

The edge triggered D flip flop has only one i/p terminal. The D flip flop has only one synchronous control i/p in addition to the clk.This is known as D input. There are two types of D flip flop.

1.'+ve'edge triggered D flip flop.
2.'-ve'edge triggered D flip flop.

Incase of '+ve' edge triggered D flip flop the o/p Q will go to the state that is present on the D i/p at the '+ve'going transition of the clk pluse.
In case of '+ve' edge triggered D flip flop operates in the same way as '+ve' edge triggered D flip flop except that the change of state takes place at the '-ve' going edge of the clk pluse.

CIRCUIT DIAGRAM:

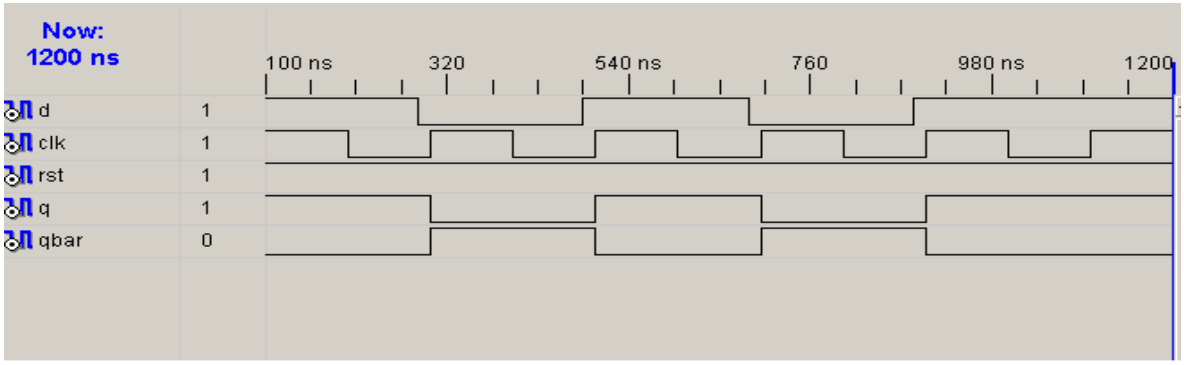
TRUTH TABLE:

D	CLK	Q	QBAR	COMMENTS
0	'+VE'	0	1	RESET
1	'+VE'	1	0	SET

PROGRAM:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity d_flip is
    Port ( D : in std_logic;
           clk : in std_logic;
           rst : in std_logic;
           Q : out std_logic;
           QBAR : out std_logic);
end d_flip;
architecture Behavioral of d_flip is
 signal state : std_logic;
begin
process(rst,clk,D)
begin
if(rst='0')then state<='0';
elsif(clk='1'and clk'event)then state<=D;
end if;
end process;
Q<=state;
QBAR<=not state;
end Behavioral;
```

WAVEFORMS:



CONCLUSIOS:

From above waveforms we observed that experimental result perfectly matched with TRUTH TABLE.

EXPERIMENT NUMBER:- Date:-

TO DESIGN AND IMPLEMENT UP/DOWN COUNTER USING VHDL.

OBJECTIVE:

i) Design of up/down counter using VHDL.

II) View and analyse the generated circuit.

THEORY:

In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. In practice, there are two types of counters:

- Up counters, which increase (increment) in value.
- Down counters, which decrease (decrement) in value.

The simplest counters use toggle flip-flops. These are made from D flip-flops as shown fig.1. This is why many circuits of counter's show an XOR gate and an AND gate for each flip-flop.

1. UP COUNTER:

CIRCUIT DIAGRAM:

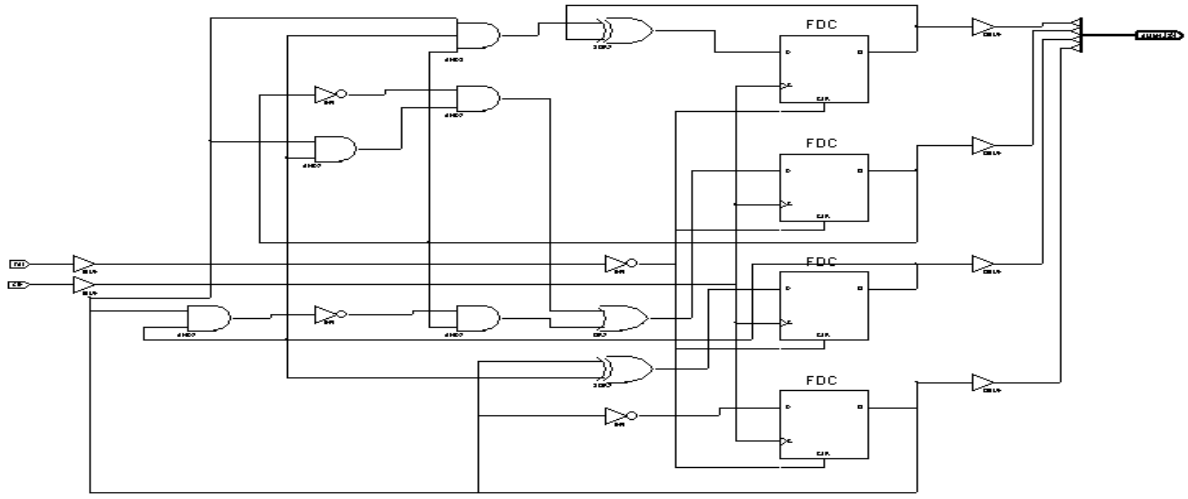
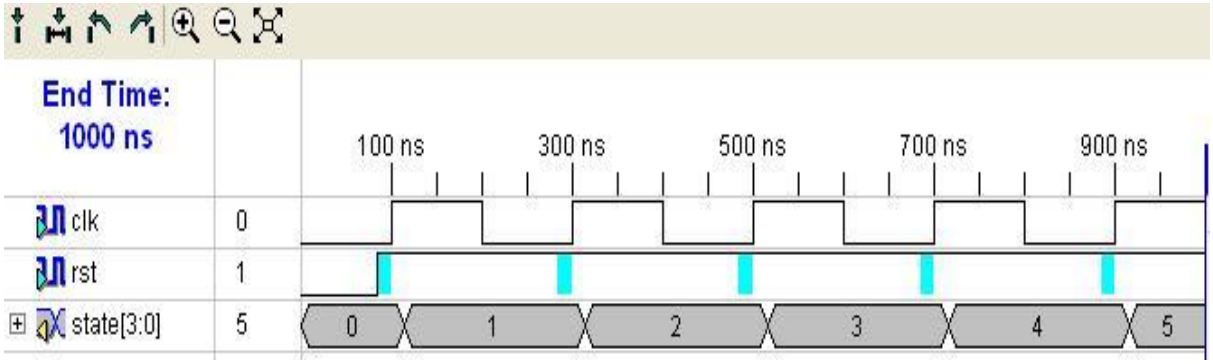


fig.1. Technology Schematic.

VHDL CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity upcounter is
    Port ( rst : in std_logic;
           clk : in std_logic;
           state : out std_logic_vector(3 downto 0));
end upcounter;

architecture Behavioral of upcounter is
signal seg:std_logic_vector(3 downto 0);
begin
process(rst,clk)
begin
if rst='0' then seg<="0000";
elsif clk='1' and clk'event then
seg<=seg+1;
end if;
end process;
state<=seg;
end Behavioral;
```

SIMULATION WAVEFORM:



2. ***DOWN COUNTER:***

CIRCUIT DIAGRAM**:**

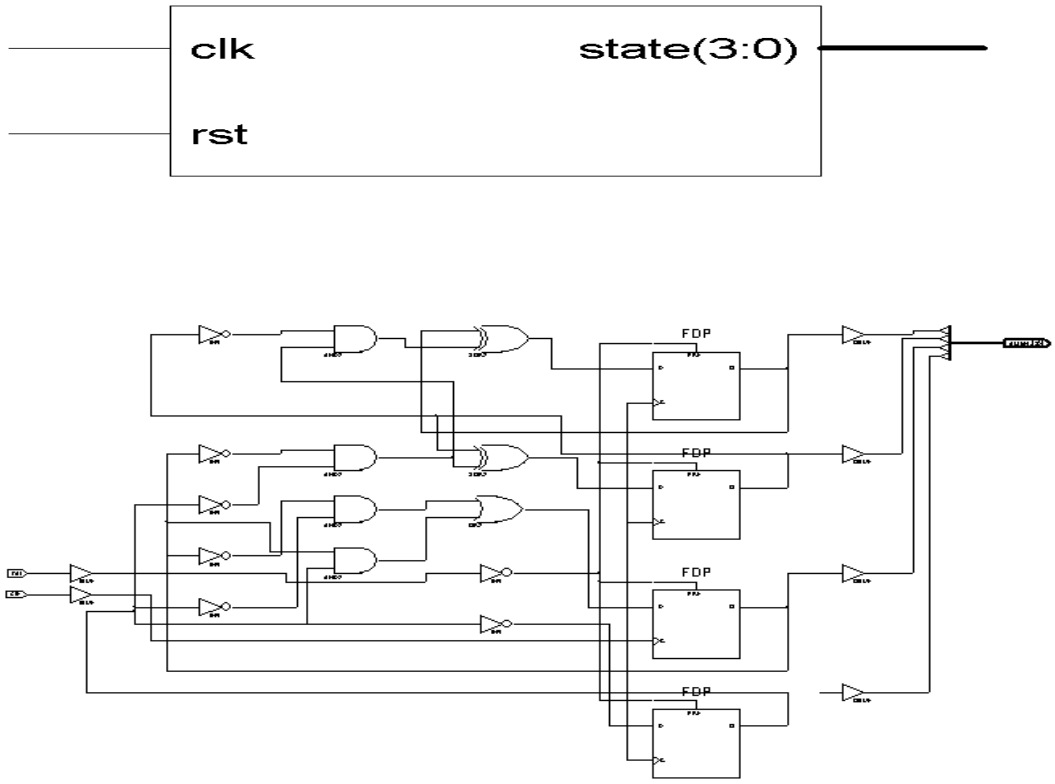


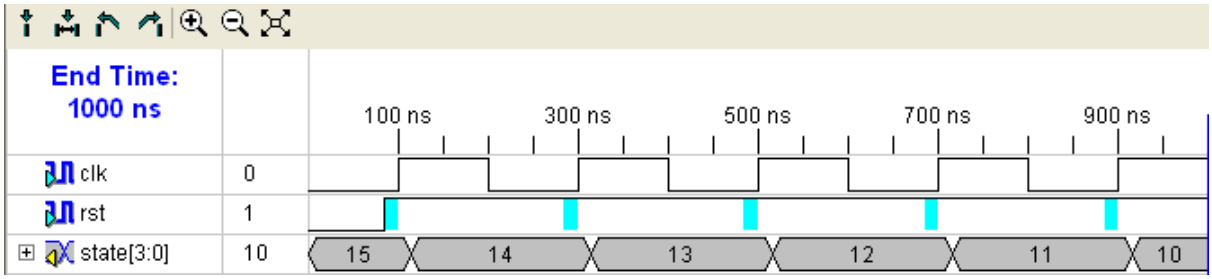
fig.2. Technology schematic

VHDL CODE:

library **IEEE;**
use **IEEE.STD_LOGIC_1164.ALL;**

```
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity downcounter is
    Port ( rst : in std_logic;
           clk : in std_logic;
           state : out std_logic_vector(3 downto 0));
end downcounter;

architecture Behavioral of downcounter is
 signal seg:std_logic_vector(3 downto 0);
begin
process(clk,rst)
begin
if rst='0' then seg<="1111";
elsif clk='1' and clk'event then
seg<=seg-1;
end if;
end process;
state<=seg;
end Behavioral;
```

SIMULATION WAVEFORM:



CONCLUSION:

Up and Down counter is a asynchronous counter .And here counting sequence in continuous sequential in nature. So there is no overlapping in between in consecutive count in 4- bit. Due to predefined less precedence delay in the VHDL simulator, it actually causes no problems. But ,in the more higher bit counter's , it may causes ambiguities like overlapping. Some counting sequence, and it is more effectively shown in the N-bit counter. From the synthesis report we can visualise about ckt's latency, clk duration, power consumtion, total delay of signal to pass through the whole ckt.

EXPERIMENT NUMBER: - Date:-

DESIGNING AND IMPLEMENTATION OF SHIFT REGISTER.

Objective:

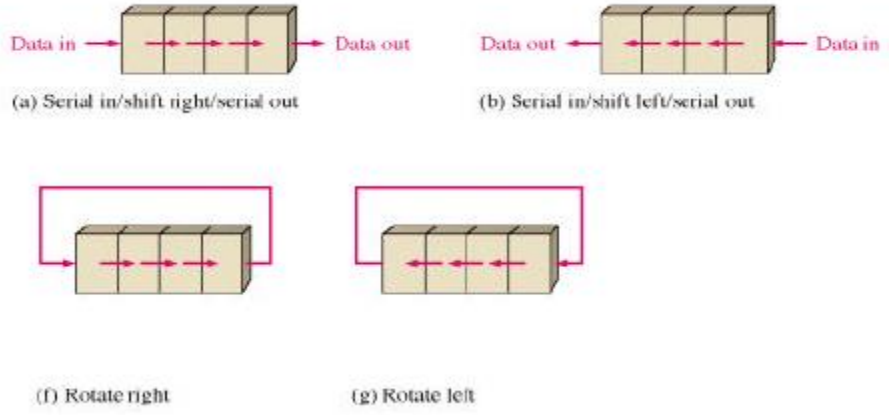
To design and implement shift registers (right, left, rotate right, rotate left)

Theory:

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flops are driven by a common clock, and all are set or reset simultaneously. They are used basically to storage and transform of digital data.

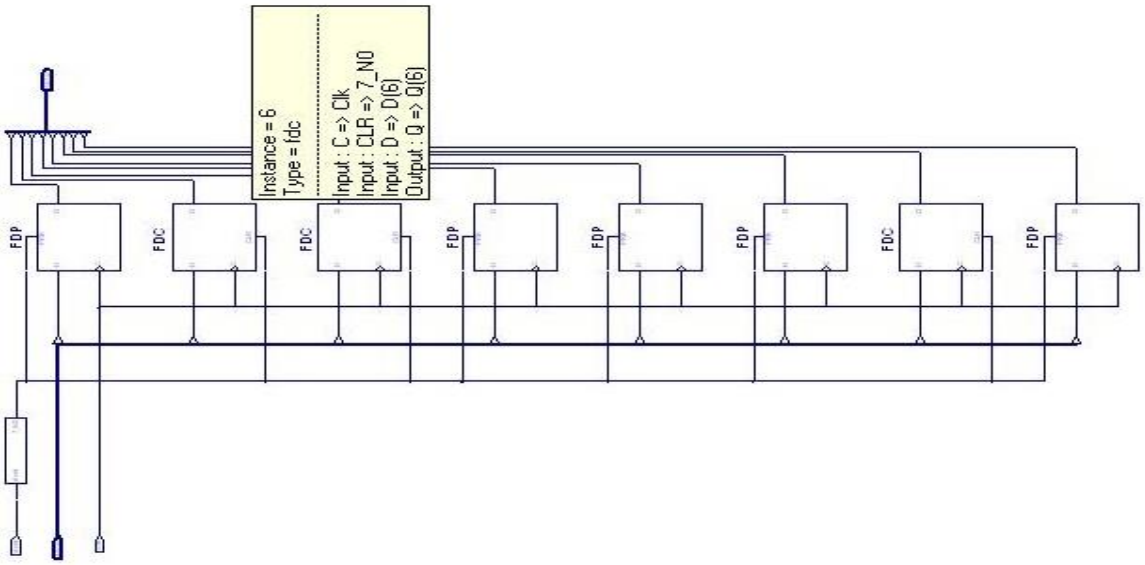
Data may be shifted in or out of the register either in serial form or in parallel form. So there are four basic types of shift registers: serial in, serial out; serial in parallel out; parallel, in serial out; parallel in, parallel out.

Here in right shift data are shifted left to right and in left shift data are shifted right to left. In case of rotate shift register data are rotated either left to right or right to left.

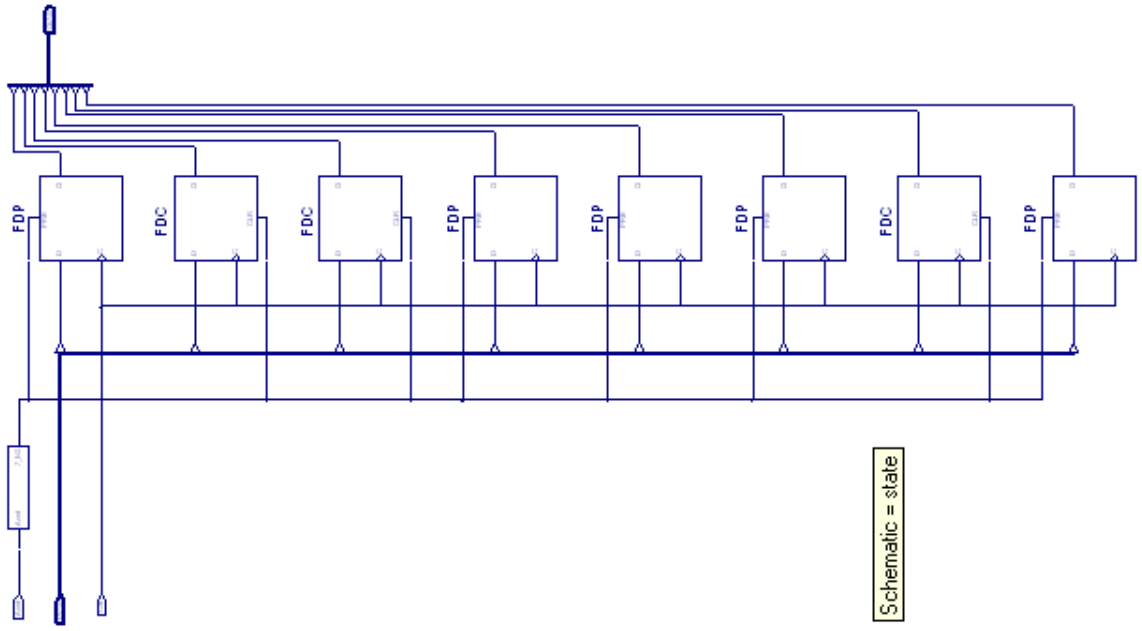


Schematic Diagram & Circuit:

(a) Right Shift Register:



(b) Left Shift Register:



Program:

(a) Right Shift Register:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entityrightshift is
    Port ( d : in std_logic;
rst : in std_logic;
clk : in std_logic;
q : out std_logic_vector(7 downto 0));
endrightshift;

architecture Behavioral of rightshift is
signalstate:std_logic_vector(7 downto 0);
begin
        process(rst,clk,d)
begin
        if(rst='0')then
        state<= "10011101";
        elsif (clk='1' and clk' event) then
        state<=d & state(7 downto 1);
        end if;
        end process;
        q<=state;
        end  Behavioral;
```

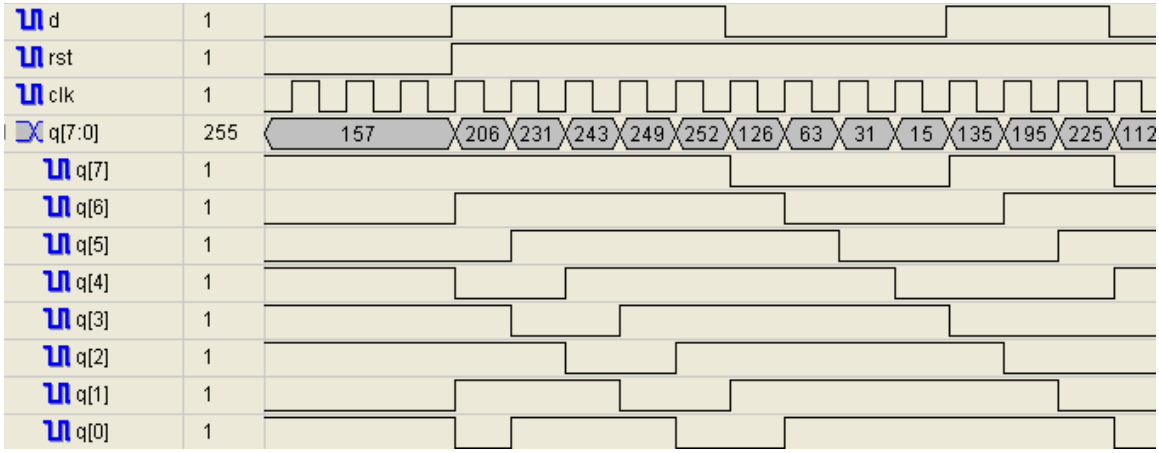
(b) Left Shift Register:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

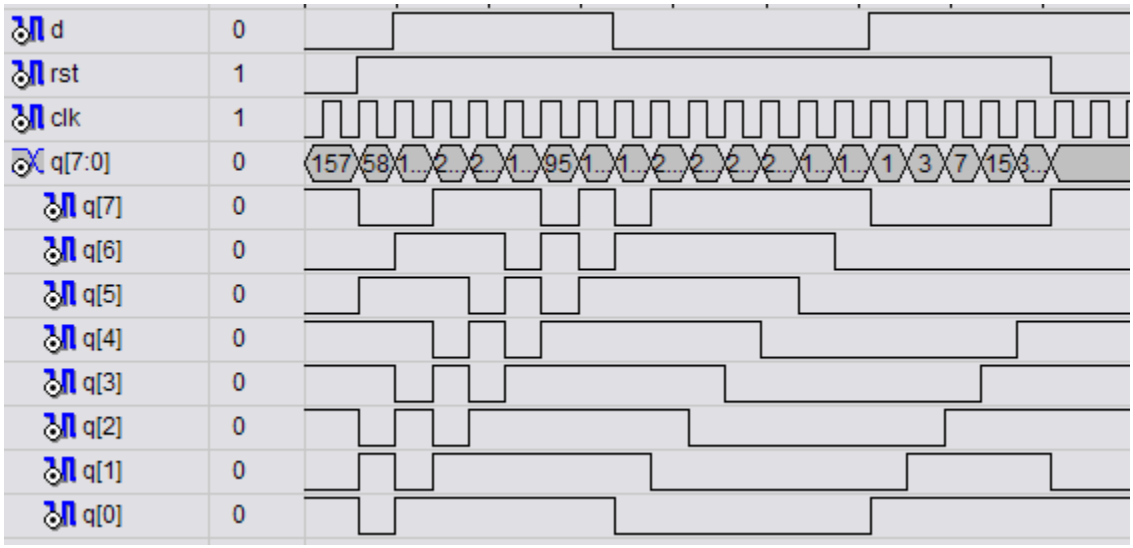
```
entityrightshift is
    Port ( d : in std_logic;
rst : in std_logic;
clk : in std_logic;
q : out std_logic_vector(7 downto 0));
endrightshift;

architecture Behavioral of rightshift is
signalstate:std_logic_vector(7 downto 0);
begin
        process(rst,clk,d)
begin
        if(rst='0')then
        state<= "10011101";
        elsif (clk='1' and clk' event) then
        state<= state(6 downto 1) & d;
        end if;
        end process;
        q<=state;
        end  Behavioral;
```

Waveform:

(a) Right Shift Register:



(b)Left Shift Register:



Conclusion:

Shift register is a very important building block. It has innumerable applications. So it is very important to know how to design it and implement a shift register. Here we have used Xlinix software to implement this circuit. This is a software part of the circuit which is later implemented on the hardware kit. In this way we can design a shift register.

CHAPTER 12: IMPLEMENTATION OF 2:4 DECODER USING XILINX ISE TOOL

Introduction:-

Discrete quantities of information are represented in digital systems with binary codes. Abinary code of n bits is capable of representing up to 2n distinct elements of the codedinformation. A **Decoder** is a combinational circuit that converts binary information from ninput lines to a maximum of 2n unique output lines. Decoder is similar to a Demultiplexerexcept that there is no data input. The only inputs are the control inputs A and B.

In this chapter, the implementation of a **2:4 Decoder** using **Xilinx ISE Tool**will be described**.**

- Write the functionality in the Xilinx project navigator.
- Run a functional HDL simulation.
- Synthesize your design with XST.
- Take the synthesized design through the Xilinx implementation tools.
- Download the bit stream file.
- Check the performance of your design by applying binary inputs and verify the outputs.

Objectives:-

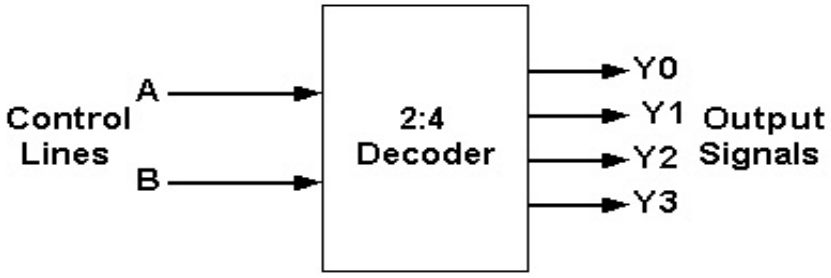
After completing this lab, student will be able to design the Decoder and validate it using CPLD/FPGAbased trainer kit.

Design Description:-

The Truth Table of 2:4 decoders is as below.

Control Lines		**Output Lines**			
A	**B**	**Y0**	**Y1**	**Y2**	**Y3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

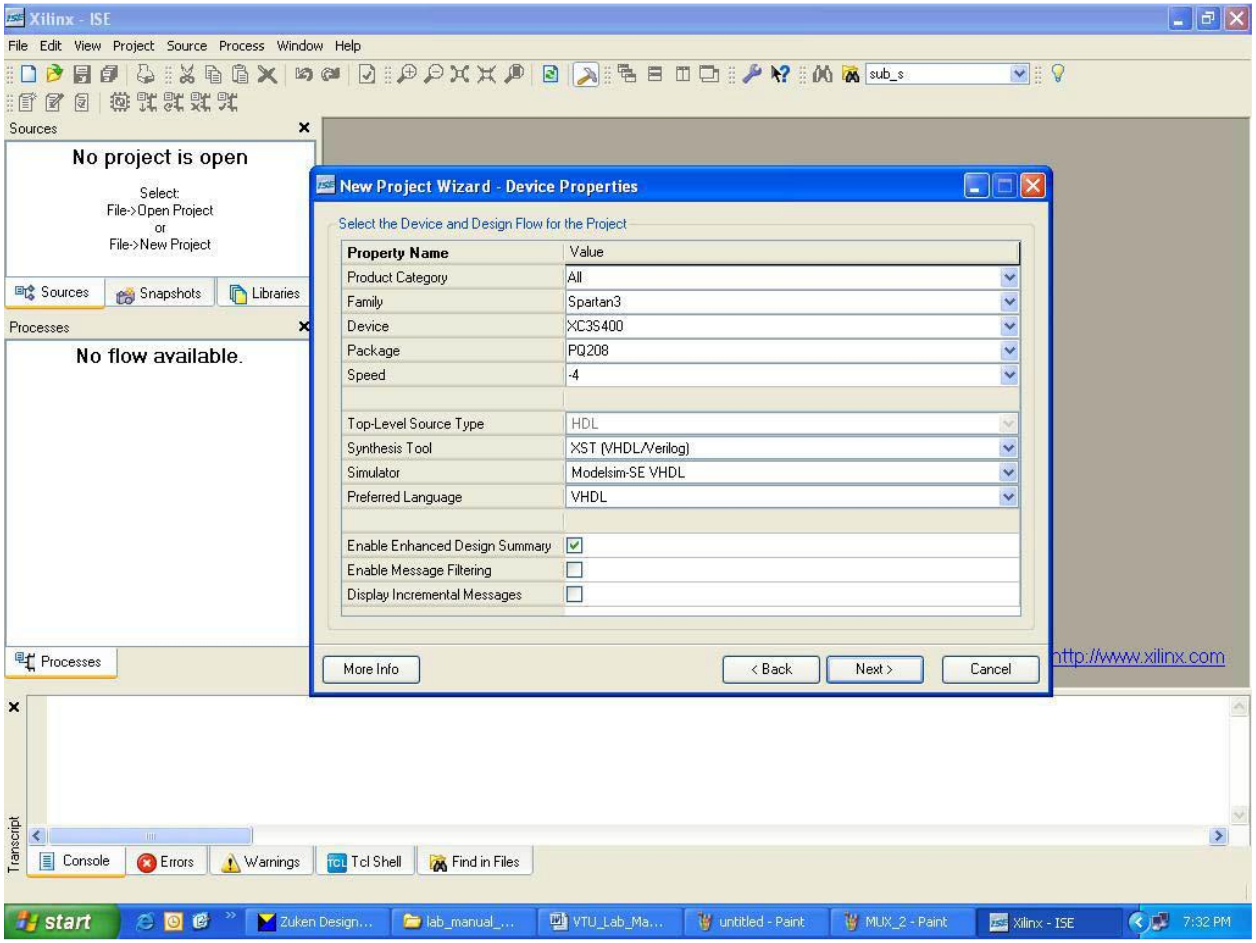
The Block Diagram of **2:4 Decoder**is as shown below.



Steps to implement the 2:4 Decoder

Step 1: Start the Xilinx Project Navigator by using the desktop shortcut or by using the Start → Programs→ Xilinx ISE→ Project Navigator

Step 2: In the Project Navigator window go to FILE → New project → Select Device.



Step 3: Click on the symbol of FPGA device and then right click → Click on new source →

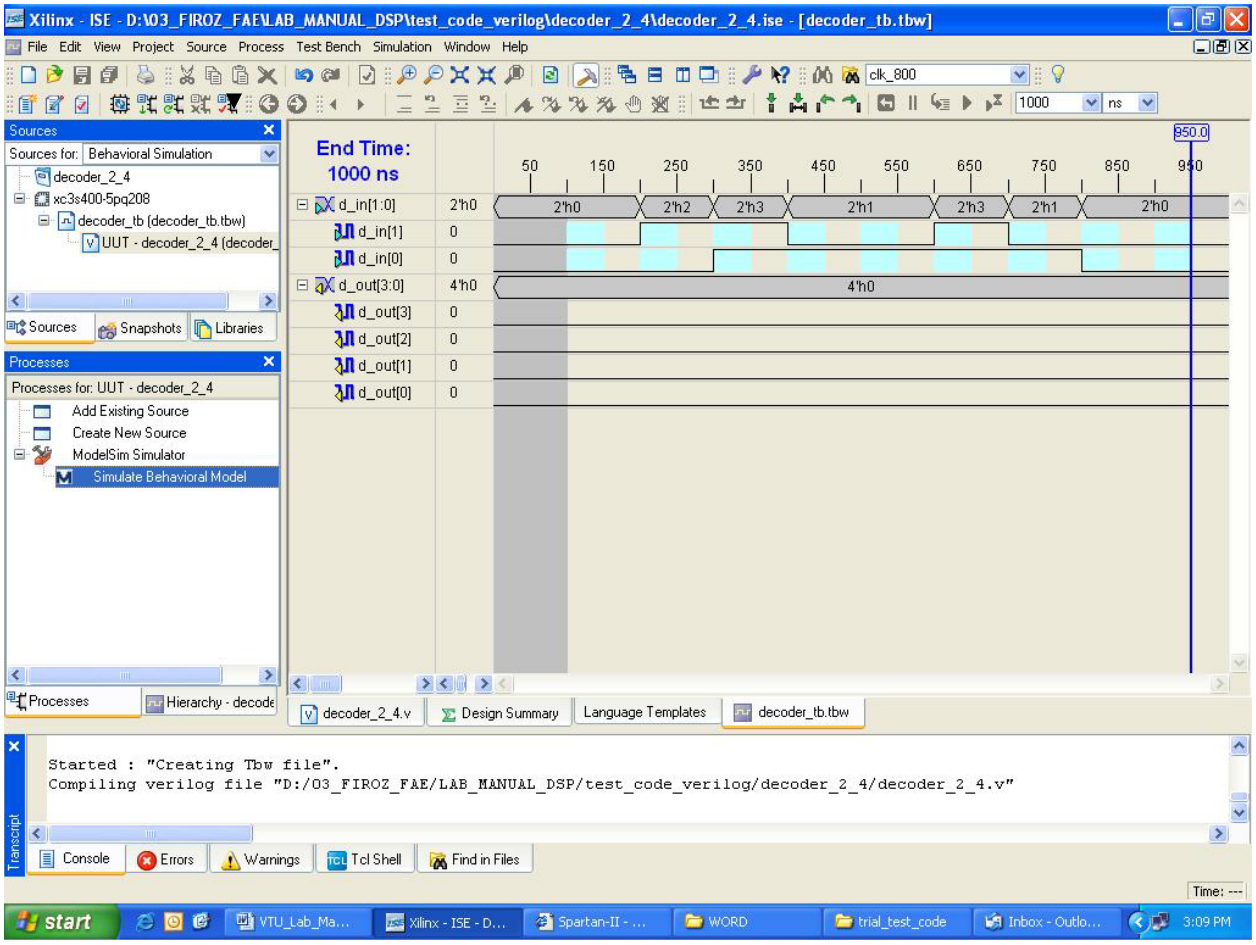
VHDL module and give the name Decoder_2_4 → Define ports → Finish.

Step 4: Generate the Behavioral VHDL Code for the Decoder_2_4.

Step 5: Check syntax, and remove errors if present.

Step 6: Simulate the design using Xilinx.

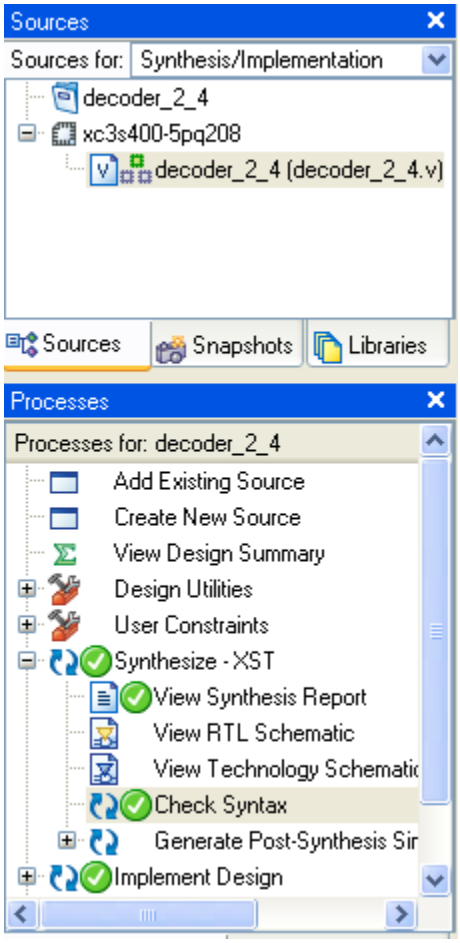
Highlight **decode2_4_tb.vhd** file in the Sources in Project window. To run the Functional Simulation, Click on the symbol of FPGA device and then right click → Click on new source → Click on test bench waveform → Give file name → Select entity → Finish → Give inputs. Click → on simulate behavioral model → see the output.



Step 7: Synthesize the design using XST.

Highlight **decode2_4.vhd** file in the Sources in Project window. To run thesynthesis, right-click on Synthesize, and choose the Run option, *or* double-click on **Synthesize** in the Processes for Current Source window. Synthesis will run,and a green check will appear next to Synthesize

when it is successfullycompleted. A yellow exclamation mark indicates that a warning was generated,and a red cross indicates an error was generated. Warnings are OK.



If there are any errors, you can view the error through the console window otherwise continue on to the next step.

Step 8: Following the procedure described in step 6 generate User Constraint file (ucf) by selecting the device in the source window and selecting the Implementation Constraints file. Select the corresponding .ucf file and open process window then select "**user constraints**" and then select "**assign pakage pin"** wherein the CPLD/FPGA package pins are oriented as per the hardware. Design object list window will appear. Select the inputs and outputs from the I/O bank. The pin configuration is given below in tabular form. In LOC field insert the required input/output pin in the format p51, p52… then click on save and OK. To edit the .ucf file click on process and then edit the constraints (test) file. The syntax is **NET "a" LOC = "p51", NET "b" LOC = "p50"**

Dedicated Pin for CPLD module (XC9572-15 PC84)

PIN NO	FUNCTION
8, 16, 27, 42, 49, 60	GND
22, 38, 64,73, 78	5V
28	TDI
29	TMS
30	TCK
59	TDO

For details interfacing the pin assignment section is referred which is included at the last of this manual.

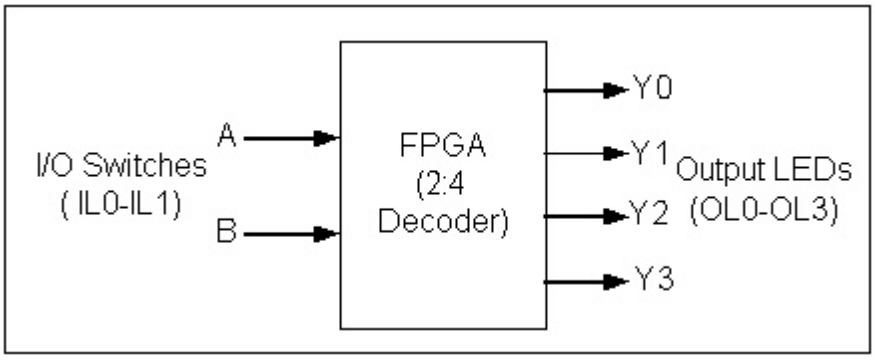
Step 9: Right-click on **Implement Design**, and choose the **Run** option, *or* double leftclickon **Implement Design.**Right-click on **Generate Programming File**, and choose the **Run** option, *or*double left-click on **Generate Programming File.** This will generate the Bitfile for FPGA or jed file for CPLD.

Step 10: Double click on **Configure Device. Impact dialog box** will appearto download the bit stream. For interfacing the target device to parallel port of computer JTAG cable is required. For CPLD device the JTAG programmer is activated while programming. Then select cable auto connect option from "xxxx" menu. The software will search for JTAG interface and display the cable connection establishment. After this user can perform various operations like erase/program/verify/ID check/ blank check from the operation menu and proceed accordingly.

For FPGA device tool will offer three options JTAG/Hardware Debugger/PROM Formatter. For downloading the design in FPGA device, user has to select "Hardware Debugger" option and then select the cable type Viz. parallel. Once the cable is sensed then download the design by using download option. If the device is configured properly the red LED given on the FPGA board will glow indicating proper configuration of the device.

Step 11: Apply input through DIP Switches and output is displayed on LEDs.

Experimental Set up:-



Conclusion:-

Design of 2:4 Decoder is implemented in Protoboard and is verified according to the truthtable.

TestCodes:-

VHDL Code for 2:4 Decoder:-

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Decoder is
Port (
D_in : in std_logic_vector(1
downto 0);
D_out : out std_logic_vector(3
downto 0));
end Decoder;
architecture Behavioral of Decoder is
begin
D_out<= "0001" when D_in = "00"
else
"0010" when D_in = "01"
else
"0100" when D_in = "10"
else
“1000”;
end Behavioral;
```

SILIGURI INSTITUTE OF TECHNOLOGY

ELECTRONICS & COMMUNICATION ENGINEERING

LABORATORY

FILE

PAPER NAME : RF & Microwave Engg Lab

PAPER CODE : EC793A

SYLLABUS

RF & Microwave Engg Lab
Code: EC793A
Contacts: 3
Credits: 2
Experiments

1. Determination of phase and group velocities in a waveguide carrying TE10 Wave from Dispersion diagram [ω−β Plot].
2. Measurement of unknown impedance using shift in minima technique using a waveguide test bench/ Measurement of thesusceptance of an inductive and or a capacitive window using shift in minima technique using a waveguide test bench
3. Study of the characteristics of a Reflex Klystron oscillator
4. Study of Gunn-oscillator Characteristics using X-band waveguide test bench.
5. Measurement of coupling factor, Directivity, Insertion loss and Isolation of a Directional coupler using X-band waveguidetest bench set up.
6. Scattering matrix of a magic tee / E-plane tee / H-plane tee using waveguide test bench at X-band.
7. Experimental/Simulation Study of filter (LPF, HPF,BPF) response.
8. Measuring of dielectric constant of a material using waveguide test bench at X-band.

LIST OF EXPERIMENT

1. Familiarization of Microwave Test Bench.
2. Determination of phase and group velocities in a waveguide carrying TE10 Wave from Dispersion diagram [ω−β Plot].
3. Measurement of unknown impedance using shift in minima technique using a waveguide test bench.
4. Study of the characteristics of a Reflex Klystron oscillator.
5. Study of Gunn-oscillator Characteristics using X-band waveguide test bench.
6. Measurement of coupling factor, Directivity, Insertion loss and Isolation of a Directional coupler using X-band waveguide test bench set up.
7. Scattering matrix of a magic tee using waveguide test bench at X-band.
8. Measuring of dielectric constant of a material using waveguide test bench at X-band.

SILIGURI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

RF & Microwave Engg LAB – EC 793A **Date:**

Experiment No.:

1(a) NAME OF THE EXPERIMENT:

Familiarisation of the X-Band Microwave Test Bench

OBJECTIVE:

- To study the overall function of X Band Microwave Test bench and different microwave components and sources.

MICROWAVE TEST BENCH

With the help of a typical X- band microwave test bench we can perform the following experiments.

1. Study of the characteristics of klystron Oscillator and to determine its electronic tuning range.
2. V-I characteristics of Gunn Diode.
3. Following characteristics of Gunn Diode Oscillator
    (i) Output power and frequency as a function of voltage
    (ii) Square wave modulation through Pin Diode.
4. To determine the standing wave ratio (swr) and reflection coefficient.
5. To measure an unknown impedance with Smith Chart.
6. Calibration of a variable Attenuator.
7. To determine the frequency & wavelength in a rectangular waveguide working on TE10 mode.
8. Square law behaviours of a microwave crystal detector.

9. To study the radiation pattern and determine different parameters of microwave antennas e.g., Slotted Broad Wall, Slotted Narrow Wall, Dielectric Antenna, H-Plane Sectorial Horn, Pyramidal Horn, Parabolic Dish etc.
10. Measurements of Dielectric constant of Low-loss solid dielectrics and Liquid dielectrics.
11. Phase shift measurements by using phase shifter.
12. Study of E Plane Tee, H Plane Tee and Magic Tee.
13. Study the function of Multihole Directional coupler by measuring the following parameters.

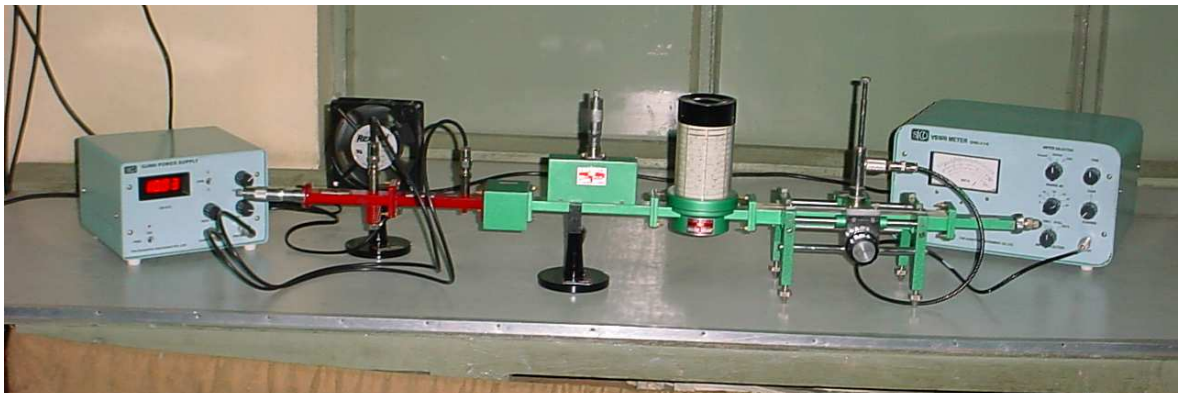


Fig: Gunn based X-band Microwave Test bench (8.2 to 12.4 Ghz)

MICROWAVE COMPONENTS

Gunn Oscillators

Gunn Oscillators are solid state microwave energy generators. These consist of waveguide cavity flanged on one end and micrometer driven plunger fitted on the other end. A Gunn-diode is mounted inside the Wave guide with BNC (F) connector for DC bias. Each Gunn oscillator is supplied with calibration certificate giving frequency vs micrometer reading.

PIN Modulators

PIN modulators are designed to modulate the CW output of Gunn Oscillators. It is operated by the square pulses derived from the TNC connector of the Gunn power supply. These consist of a PIN diode mounted inside a section of Wave guide flanged on its both end. A fixed attenuation vane is mounted inside at the input to protect the oscillator.

Klystron Mount

Klystron mounts are used to transmit microwave power from reflex klystron tube to rectangular waveguide. Klystron mounts are designed by a section of waveguide, one end of waveguide is fitted with a movable short plunger. A small hole on the broad wall of waveguide is provided through which coupling pin of reflex klystron tube enters into the waveguide. By moving plunger (matching the impedance of klystron tube and waveguide) maximum output can be achieved.

Isolators

The ferrites isolators and circulators are matched 2 port and 3 port devices respectively, which offer low insertion loss and high isolation over 1GHz band width. An isolator is a 2 port device which allows signals from port 1 to port 2 & provides maximum attenuation for transmission from port 2 to 1. A circulator is a three port device which has a peculiar property of coupling power to the adjacent port clockwise.

Fixed Attenuators

Attenuators are required to adjust power or attenuate the power flowing in waveguide. There are two types of attenuators fixed and variable. Fixed attenuators are available in various range like 3dB, 6dB, 10 dB etc. These attenuators are calibrated at center frequency of respective frequency band. By Variable attenuators power can be adjusted for different level.

Variable Attenuator (10 Db/20 Db)

Direct Reading Frequency Meter

Direct Reading frequency meters are used to measure the microwave frequency accurately. There long scale length and numbered calibration marks provide high resolution which is particularly useful when measuring frequency difference of small frequency changes.

Slotted Section

Slotted section is used to measure various measuring parameter in microwave, for example to determine standing wave pattern, VSWR, phase and impedances. These consist of a slot in center of waveguide in which we can connect a probe and probe can be moved in slot and position of probe can be measured by its Varnier scale. The travel of probe carriage is more than three times of half wavelength.

Tunable Probe

Tunable probes are very useful devices to measure the SWR and Impedances. Tunable probe is consists of a crystal detector and a small wire antenna in coaxial housing. Its depth of penetration into the slotted section is variable.

Matched Termination

Matched terminations are used to terminate the waveguide transmission line operating at low average power. The loads are carefully designed to absorb all the applied power and VSWR of matched termination is low. These are used in the measurement of reflection coefficient and where the matched load is required.

Wave Guide Detector Mount

The crystal detector can be used for the detection of microwave signal. At low level of microwave power, the response of each detector approximates to square law characteristics and may be used with a high gain selective amplifier having a square law meter calibration.

Slide Screw Tuners

Slide Screw Tuner is a very useful component in a microwave laboratory. It is mainly used for Impedance measurement. Its tuner can be adjusted for low and high impedance position.

E-Plane and H-plane Bends

In measurements it is often necessary to bend a waveguide by some angle. Waveguide bends in E and H plane of 90° is normally available. Waveguide bends are designed by a section of rectangular waveguide and flange.

Multihole Directional Coupler

Directional coupler are designed to measure incident and reflected power values and also provide a signal path to a receiver or perform other desirable operation. In its most common form, the directional coupler is a four fort waveguide junction consisting of a primary main waveguide and a secondary auxiliary waveguide. These are available in 3, 6,10, 20, 40 dB coupling.

Cross Directional Coupler

Cross Directional Coupler consists of two waveguide sectional joint at (90°) with the coupling element mounted into the common broad wall.

Tee

Tees are used to combine power from two inputs or divided the microwave power from one input to two output lines. Tee is an intersection of three waveguides in the form of alphabet T.

E Plane Tee and H Plane Tee

Magic Tee or E-H Tee

Waveguide Antennas

There are several types of microwave antennas like standard Gain, Pyramidial horn, Pick up horn, Dielectric antenna, Parabolic dish antenna etc. these are used to radiate microwave energy in the air and to receive the energy from air.

Precision Movable Short

Movable shorts are used to obtain a phase reference in the calibration of various experimental setups .These are also used to vary the effective plane of reflection and therefore the phase of reflected wave. Movable shorts are used to measure the impedance of a device. Movable shorts are of two types one has no provision to record position of short in the waveguide and other type of movable short is precision movable short in which position of short can be accurately recorded from micrometer.

Phase Shifter

Many applications require phase shift to be introduced between two given position in a waveguide system. It consists of a dielectric slab or vane specially shaped to minimize reflection effect. Phase shifter is used to change the effective electrical length of transmission line without changing its physical length. They are particularly useful in microwave bridge circuit where the phase and amplitude must be adjusted independently.

REVIEW QUESTIONS

What is microwave?

List some microwave frequency bands.

List some of characteristic feature of microwave.

List some of the application of microwave technology.

Draw a simple microwave system.

What are waveguide `Tees'?

List the basic type of waveguide tees.

What is an isolator?

What is a circulator?

What is a directional coupler?

What is velocity modulation?

Mention the Principle used in Klystron?

When the o/p power of reflex klystron maximum?

What is meant by attenuator?

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Experiment No.: 1

AIM: Measurement of wavelength, guided wavelength and frequency using waveguide test bench. Calculation of broad wall dimension of waveguide and ω-β plot.

OBJECTIVES:

1. To determine the Frequency (f_o) and wavelength (λ_0) and guided-wavelength (λ_g) of a microwave source in a rectangular waveguide on TE_{10} mode.

2. To plot the ω-β diagram.

APPARATUS USED:

Sr. No.	Name of the equipment	Quantity	Range/Rating	Make
1.	Reflex Klystron/Gunn	1	X – Band	SICO/ScienTech
2.	Oscillator	1	-do-	-do-
3.	Klystron Power	1	-do-	-do-
4.	Supply/Gunn Power	1	-do-	-do-
5.	Supply	1	-do-	-do-
6.	Pin Modulator	1	-do-	-do-
7.	Isolator	1	-do-	-do-
8.	Variable Attenuator	1	-do-	-do-
9.	Frequency Meter	1	-do-	-do-
10.	Slotted Section	1	-do-	-do-
11.	Tunable Probe	1	-do-	-do-
12.	VSWR Meter	1	-do-	-do-
	Movable Short			
	CRO			

THEORY:

For dominant TE10 mode in rectangular wave-guide λ_0, λ_g and λ_c are related as below.

$$1/\lambda_0^2 = 1/\lambda_g^2 + 1/\lambda_c^2$$

Where λ_0 is free space wavelength

λ_g is guide wavelength

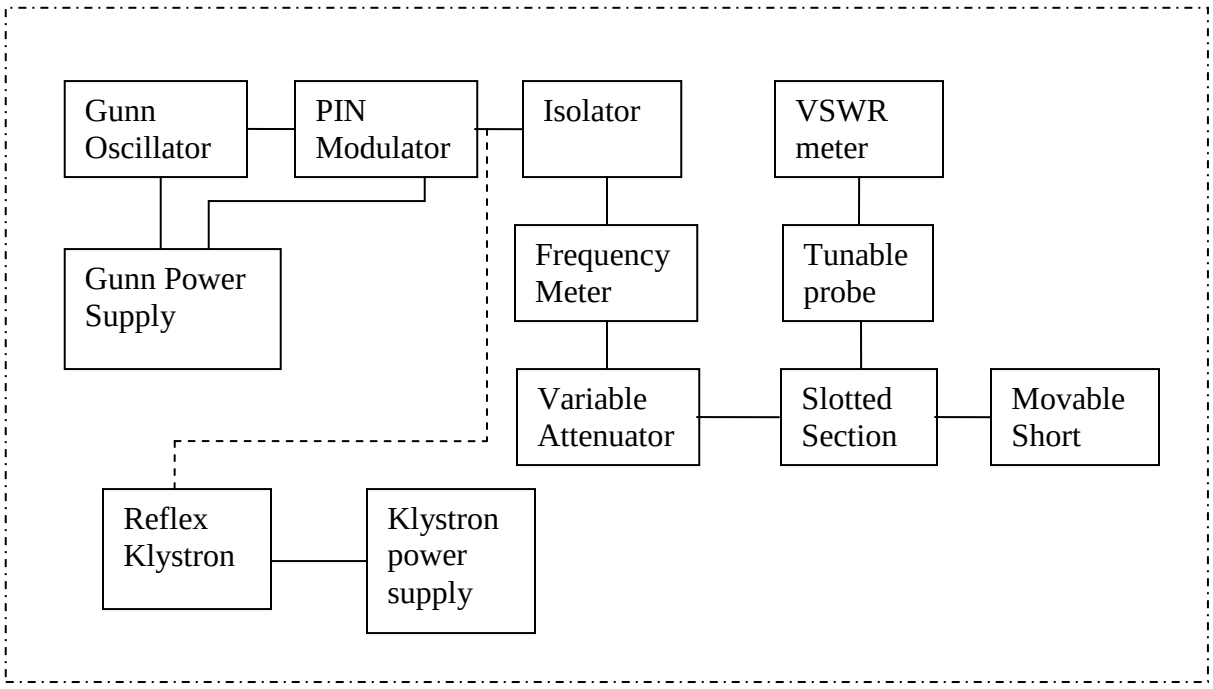
λ_c is cutoff wavelength

For TE10 mode, $\lambda_c = 2a$ is broad wall dimension of waveguide. The following relationship can be proved

$$f = c/\lambda = c\sqrt{(1/\lambda_g^2 + 1/\lambda_c^2)}$$

Where c is velocity of light and f is frequency.

EXPERIMENTAL SETUP:



PROCEDURE:

1. Set up the components and equipments as shown in fig. 1.
2. Set the variable attenuator at maximum position.
3. Keep the control knobs of VSWR meter as below: -

Range db	--	50 db position
Input switch	--	Crystal Low Impedance
Meter switch	--	Normal Position
Gain (Coarse &Fine)	--	Mid Position

4. Keep the Control knobs of Klystron power supply as below

Meter Switch	--	OFF
MOD-Switch	--	AM
Beam Voltage Knob	--	Fully anti clockwise
Repeller Voltage	--	Fully clockwise
AM Amplitude Knob	--	Around fully clockwise
Mod Frequency Knob	--	Around Mid Position

5. Switch on the Klystron Power Supply, VSWR Meter and Cooling Fan.
6. Turn the meter switch of the power supply to beam voltage position and set the beam voltage at 300 volts with the help of beam voltage control knob.
7. Adjust the repeller voltage to some deflection in the VSWR Meter.
8. Maximize the deflection with AM amplitude and frequency control knob of power supply.

9. Tune the plunger of Klystron Mount for maximum deflection.
10. Tune the repeller voltage knob for maximum deflection.
11. Tune the probe for maximum deflection in VSWR meter.
12. Tune the frequency meter knob to get a 'dip' on VSWR scale and note the frequency directly from the frequency meter
13. Replace the termination with movable short and detune the frequency meter.
14. Move the probe along the slotted line, the deflection in the VSWR meter will vary. Move the probe to a minimum deflection position. To get accurate reading, it is necessary to increase the VSWR meter range dB switch to higher position. Note and record the probe position.
15. Move the probe to next minimum positions and record the probe positions.
16. Calculate the guide wavelength as twice the distance between two successive minimum positions obtained as above.
17. Measure the wave-guide inner broad wall dimension 'a' which will be around 22.86 mm for X- band.
18. Calculate the frequency by following equation:

$$f = c/\lambda = c\sqrt{(1/\lambda_g^2 + 1/\lambda_c^2)}$$

Where $c = 3x10^8$ meter /sec. i.e. velocity of light.

19. Verify the frequency obtained by frequency meter.
20. Plot the graph between $\omega(= 2\pi f)$ *and* $\beta(= 2\pi/\lambda_g)$.
21. The above experiment can be verified at different frequencies.
22. If the Gunn oscillator and PIN modulator is used instead of Klystron operating procedure of Gunn oscillator is to be followed.

Observation Table:

Sl. No. of Obs	Frequency meter reading (GHz)	Probe position at minima (cm)				$\lambda_g/2$ (cm)			Av. λ_g (cm)	λ_0 (cm)	f_0 GHz	ω	β
		m_1	m_2	m_3	m_4	$(m_1 \sim m_2)$	$(m_2 \sim m_3)$	$(m_3 \sim m_4)$					
1.													
2.													
3.													
…													
…													
…													

CALCULATION AND RESULTS:

CONCLUSION:

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Experiment No.: 2

AIM: Measurement of Unknown Impedance (inductive, capacitive and resonant windows).

OBJECTIVE:To measure the input impedance of a terminated waveguide using shift in minima technique and smith chart.

APPARATUS USED:

Sr. No.	Name of the equipment	Quantity	Range/Rating	Make
1.	Reflex Klystron/Gunn Oscillator	1	X – Band	SICO/ScienTech
2.	Klystron Power Supply/Gunn Power Supply Pin Modulator	1	-do-	-do-
3.	Isolator	1	-do-	-do-
4.	Variable Attenuator	1	-do-	-do-
5.	Frequency Meter	1	-do-	-do-
6.	Slotted Section	1	-do-	-do-
7.	Tunable Probe	1	-do-	-do-
8.	S.S. tuner with matched termination/Load	1	-do-	-do-
10.	VSWR Meter	1	-do-	-do-
11.	Short	1	-do-	-do-
12.	CRO	1	0 – 20 MHz	
13.	Cooling fan	1		

THEORY

At very high frequencies, it is difficult to measure current and voltage because measuring devices become significant in size and every circuit becomes a transmission line. The slotted line is simple device used in determining the impedance of an unknown load at high frequencies up into the region of gigahertz. It can consist of a section of a rectangular waveguide with a slotted line along the mid of broadside where a detector probe can sample the E field and consequently measures the potential difference between the probe and its outer shield.

The slotted line is primarily used in conjunction with the Smith chart to determine the standing wave ratio *s*(the ratio of maximum voltage to the minimum voltage) and the normalized load impedance $\not{Z}_L$.The value of *s* is read directly on the VSWR meter when the load is connected. To determine $\not{Z}_L$, we first find the position of the load by replacing the load by a short circuit and noting the locations of voltage minima (which are more accurately determined than the maxima because of the sharpness of the turning point) on the scale attached to the slotted line. Since the impedances repeat every half wavelength, any of the minima is selected as the reference point. We now determine the distance from the selected reference point to the load by replacing the short circuit by the load and noting the locations of voltage minima. The distance d_{min} (distance of V_{min} toward the load) expressed in terms of λ (wave length) is used to locate the position of the load of an *s*– circle on the chart as shown in figure 2. We could also locate the load by using d_{min}, which is the distance of V_{min} toward the generator. Either d_{min} or $d_{min}^{/}$may be used to locate $\not{Z}_L$. Detailed steps for the impedance measurement of an unknown load using Smith chart are given in the PROCDURE chapter.

The value of normalized impedance of the load obtained with the help of Smith chart can be computed by using following important relations.

$$|\Gamma_L| = \frac{s-1}{s+1} \qquad \text{----------} \quad (1)$$

$$\Gamma_L = |\Gamma_L| \angle \phi_L \qquad \text{----------} \quad (2)$$

$$\phi_L = 2\beta d_{\min} - \pi \quad \text{----------} \quad (3)$$

$$\beta = \frac{2\pi}{\lambda_g} \quad \text{----------} \quad (4)$$

$$\bar{Z}_L = \frac{Z_L}{Z_O} = \frac{1+\Gamma_L}{1-\Gamma_L} \quad \text{----------} \quad (4)$$

$$Z_L = Z_O \frac{1+\Gamma_L}{1-\Gamma_L} \quad \text{----------} \quad (5)$$

where, Γ_L is the complex Reflection coefficient of the complex load impedance Z_L with the phase angle ϕ_L .

$\bar{Z}_L$ =normalized impedance of the load

Z_L = load impedance.

Z_O = characteristics impedance of wave guide at an operating frequency corresponding to the guided wavelength λ_g and free space wavelength λ_O .

λ_g = 2(distance between two successive minima or maxima)

Z_O may be calculated for TE_{10}mode as

$$Z_O = 377 \frac{b}{a} \sqrt{\frac{\mu_r}{\varepsilon_r}} \frac{\lambda_g}{\lambda_o}$$

a = 2.286 cm (broad-wall dimension of the x-band rectangular waveguide)

b = 1.016 cm (narrow-wall dimension of the x-band rectangular waveguide)

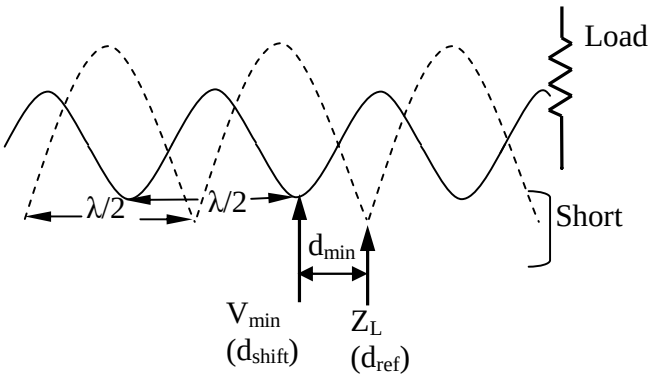


Fig1: Determining the location of the load Z_L and V_{min} on the.

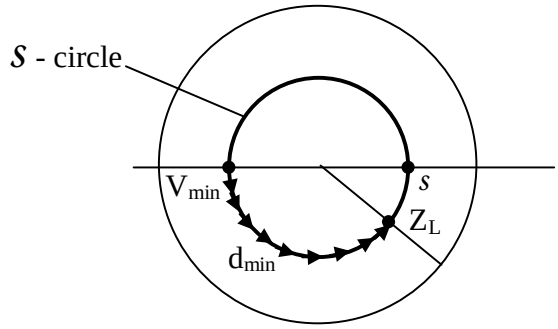
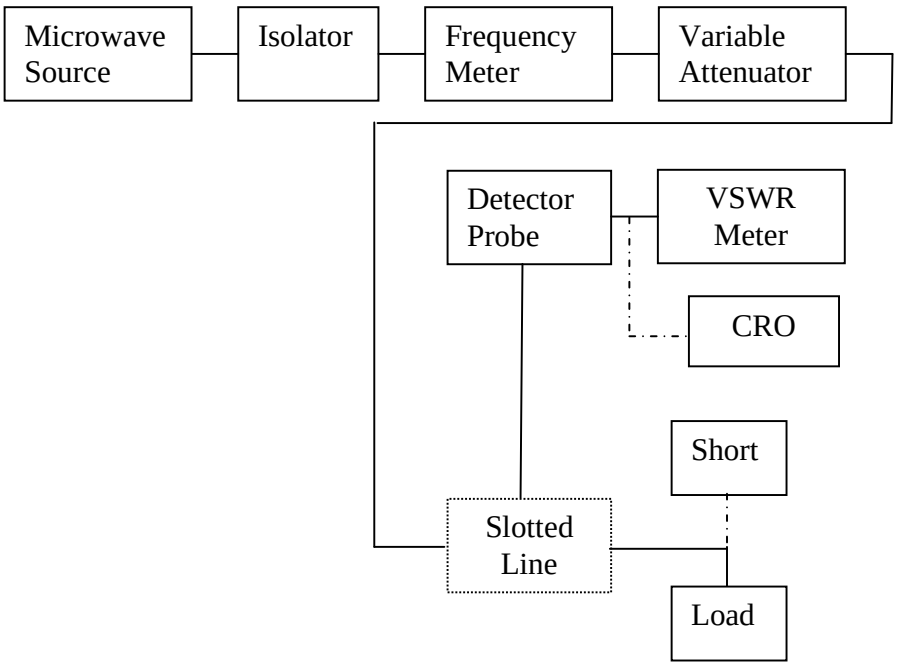


Fig2: Determination of the Load impedance from the Smith chart using the data obtained from the slotted line.

Experimental Setup:



PROCEDURE:

1. Connect the equipment as shown in the set up
2. Set the variable attenuator at maximum position.
3. Keep the control knobs of VSWR meter as below.

Range dB	:	50 dB position
Input Switch	:	Crystal low impedance
Meter Switch	:	Normal Position
Gain (Coarse & fine)	:	Mid Position.

4. Keep the Control knobs of Klystron power supply as below

Meter Switch	--	OFF
MOD-Switch	--	AM
Beam Voltage Knob	--	Fully anti clockwise
Repeller Voltage	--	Fully clockwise
AM Amplitude Knob	--	Around fully clockwise
Mod Frequency Knob	--	Around Mid Position

5. Switch ‘ON’ the Klystron power supply, VSWR meter and cooling fan.
6. Turn the meter switch of power supply to beam voltage position and set the beam voltage at 300V with the help of beam voltage knob.
7. Adjust the reflector voltage to get some reflection in VSWR meter.
8. Maximize the deflection with AM amplitude and frequency control knob of power supply.
9. Tune the reflector voltage knob for maximum deflection in VSWR meter.

10. Tune the probe for maximum deflection in VSWR meter.
11. Tune the Frequency meter knob to get dip on the VSWR scale, and note down the frequency directly from frequency meter.
12. Connect a short circuit to the slotted line. Note down the positions ofsuccessive minima on the slotted line with the help of vernier scale attached to it. Take the first minima (near to the short) as the reference point. Let it be d_{ref}.
13. Replace the short circuit with the S.S. tunerand Matched Termination.
14. Keep the depth of S.S. Tuner to around 3-4 mm and lock it.
15. Move the probe toward the generator and locate the position of the shifted minima point. Let it be d_{shift}. Then shift in minima, $d_{min}= d_{shift} - d_{ref}$.
16. Move the probe along the slotted line toward generator to get maximum deflection on the VSWR meter.
17. Adjust VSWR meter gain control knobs and if required variable attenuator such that the meter indicates 1.0 on the normal upper SWR scale.Now move the probe toward generator to get minimum deflection (dip) on the meter. Note down the SWR = Son the scale.
18. Remove the S.S. Tuner and Matched Termination and place movable short at slotted line. The plunger of short should be at zero.
19. Note the position of two successive minima position. Let it be as $d_1$andd_2 . Hence $\lambda_g= 2(d_1- d_2)$
20. Calculate d_{min} / λ_g
21. Find out the normalized impedance as described in the theory section.
22. Repeat the same experiment for other frequency if required.

[SUMMRY: The measurement is performed in following way:

1. With the load (unknown impedance) connected to the slotted line, read Son the VSWR meter. With the value of S, draw the S-circle on the Smith chart.
2. With the load replaced by a short circuit, locate a reference position for $Z_L$at a voltage minimum point.
3. With load on the line, note the position of V_{min} and determine d_{min}.

4. On the Smith chart, move toward the load a distance d_{min} (from the location of V_{min} Find the $\not{Z}_L$at that point.
5. Check the result obtained by Smith chart with the calculated value through standard formulas.]

Observation table:1

Sl. No. of Obs	**Probe position at minima (cm)**									**$\lambda_g/2$ (cm)**		**Av. λ_g (cm)**	**λ_0 (cm)**	**f_0 (GHz)**
	m_1			m_2			m_3			**($m_1 \sim m_2$)**	**($m_2 \sim m_3$)**			
	m_1'	m_1''	Avg m_1	m_2'	m_2''	Avg m_2	m_{13}'	m_3''	Avg m_3					

Observation table:2

d_{ref} (cm)	d_{shift} (cm)	d_{min} (d_{ref}- d_{shift}) (cm)	d_{min} (d_{min}/ λ) (λ)	SWR = S	$\not{Z}_L$	Z_L (Ω)

CONCLUSION

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Experiment No.: 3

AIM: KLYSTRON CHARACTERISTICS (static method and Dynamic Method) using power meter with bolometer and frequency meter.

OBJECTIVES:

(i) To study the variation of output power of a Reflex Klystron with the repeller voltage.

(ii) To study the variation of frequency of a Reflex Klystron with the repeller voltage.

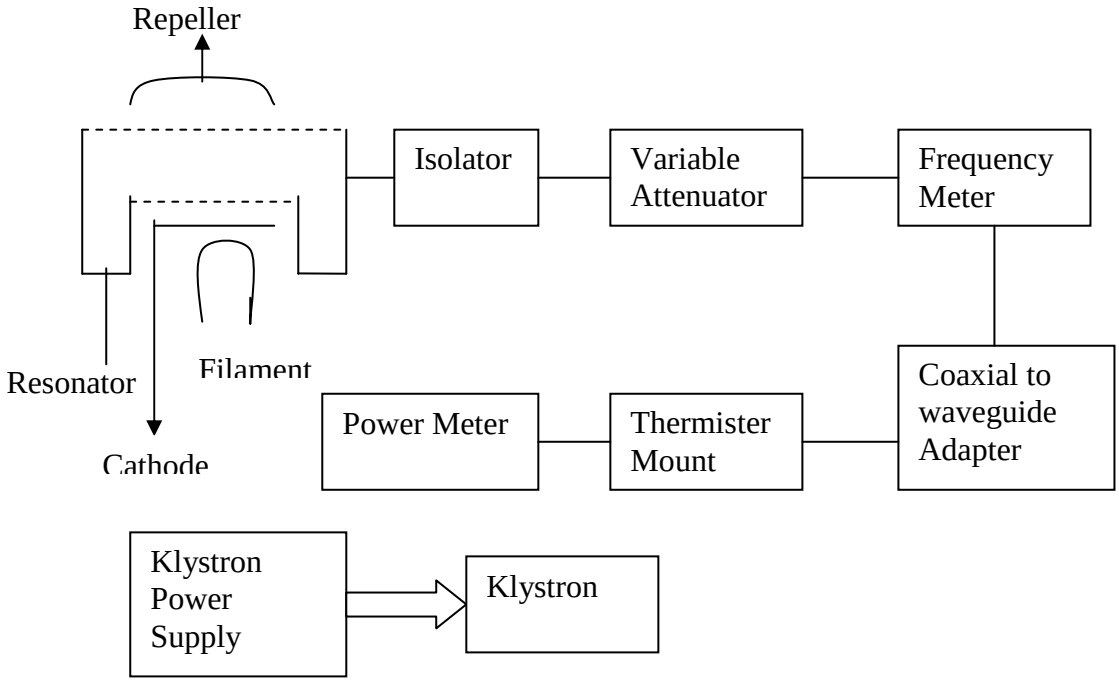
APPARATUS USED:

Sr. No.	Name of the equipment	Quantity	Range/Rating	Make
1.	Reflex Klystron	1	X – Band	SICO/ScienTech
2.	Klystron Power	1	-do-	-do-
3.	Supply	1	-do-	-do-
4.	Isolator	1	-do-	-do-
5.	Variable Attenuator	1	-do-	-do-
6.	Frequency Meter	1	-do-	-do-
	Coaxial to Waveguide			
7.	Adapter	1	-do-	-do-
8.	Thermister mount	1	-do-	-do-
9.	Power Meter	1	-do-	-do-
	Oscilloscope			

THEORY:

The Reflex Klystron makes the use of velocity modulation to transform a continuous electron beam into microwave power. Electrons emitted from the cathode are accelerated and passed through the positive resonator towards negative reflector, which retards and, finally reflects the electrons and the electrons turns back through the resonator. Suppose an RF field exists between the resonators the electrons traveling forward will be accelerated or retarded, as the voltage at the resonator changes in amplitude. The accelerated electrons leave the resonator at an increased velocity and the retarded electrons leave at the reduced velocity. The electrons leaving the resonator will need different time to return, due to change in velocities. As a result, returning electrons group together in bunches. As the electron bunches pass through resonator, they interact with voltage at resonator grids. If the bunches pass the grid at such a time that the electrons are slowed down by the voltage then energy will be delivered to the resonator; and Klystron will oscillate. The frequency is primarily determined by the dimensions of resonant cavity. Hence, by changing the volume of resonator, mechanical tuning of Klystron is possible. Also, a small frequency change can be obtained by adjusting the reflector voltage. This is called electronic tuning.

SCHEMATIC BLOCK DIAGRAM: The waveguide test bench is arranged as shown below.



PROCEDURE:

1. Connect the components and equipments as shown in the figure.
2. Set the attenuator at the maximum position.
3. Set the Mode Switch of Klystron Power Supply to CW position, beam voltage control knob to full anti-clock wise and reflector (repeller) voltage control knob to full clock wise and the Meter Switch to 'OFF' position.
4. HT ON/OFF Switch to OFF position (SICO Model only).
5. Rotate the knob of frequency meter at one side fully.
6. Put the power meter in 10 mW range.
7. Switch on the power meter and set power display to zero reading with the help of coarse and fine control.
8. Switch on the Klystron Power Supply and cooling fan.
9. Put the HT ON/OFF Switch to ON position.
10. Put the meter switch of KPS to beam voltage position and rotate beam voltage knob clockwise slowly up to 300 volts reading. Observe beam current on the meter by changing the meter switch to current position. "**The beam current should not increase more than 30 mA."**
11. Keep the meter switch of KPS at Repeller position.
12. Change the reflector voltage slowly from maximum negative value to -75 volts in steps of 5 volts. Record the repeller voltage, output power and frequency in the observation table. The frequency is measured by tuning the frequency meter to have a dip in the output each time
13. The frequency meter should be detuned each time while measuring power.
14. Plot power/frequency versus repeller voltage to get mode curves.

OBSEVATION TABLE: --

REPELLER VOTAGE Vs POWER OUTPUT and FREQUENCY

Repeller Voltage (volts)	Output power (mW)	Frequency (GHz)
-250	…	…
-245	…	…
…	…	…
…	…	…
-80	…	…
-75	…	…

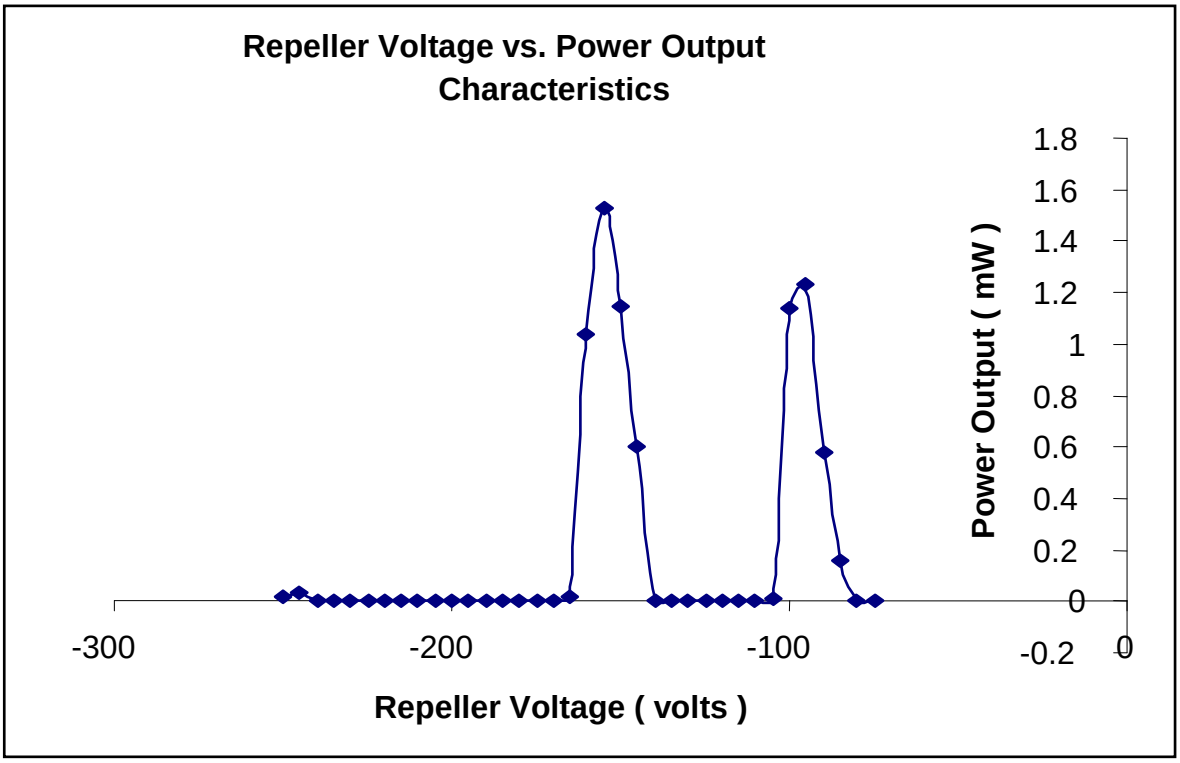


Fig: 1 . Frequency vs Power Output Characteristics Curve (sample)

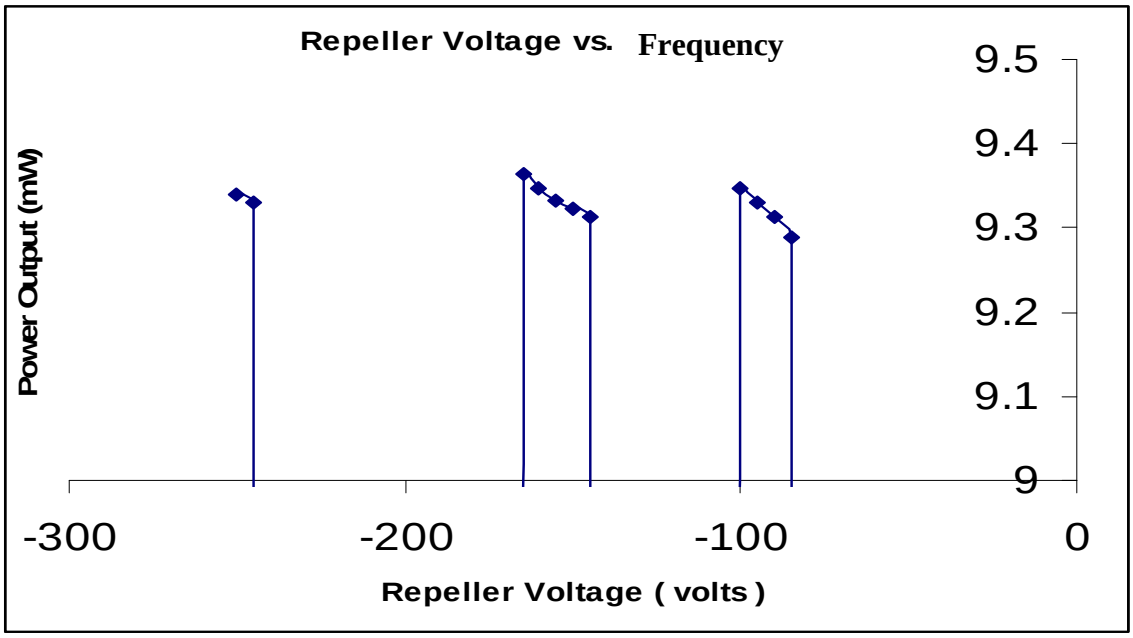


Fig (2) :--Repeller Voltage vs. Frequency Characteristics Curve (sample)

CONCLUSION: -

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Experiment No.: 4

AIM: Study of Characteristics of Gunn Oscillator using power meter with bolometer and frequency meter

OBJECTIVES:

(i) To study the characteristics of a Gunn diode oscillator by finding threshold voltage V_{th} and corresponding maximum current from the plot of bias voltage vs. diode current.

(ii) To plot the power output vs. frequency at bias voltage of 10 V.

APPARATUS USED:

Sr. No.	Name of the equipment	Quantity	Range/Rating	Make
1.	Gunn Oscillator	1	X – Band	SICO/ScienTech
2.	Isolator	1	-do-	-do-
3.	PIN Modulator (if modulated output required)	1	-do-	-do-
4.	Variable Attenuator	1	-do-	-do-
5.	Frequency Meter	1	-do-	-do-
6.	Coaxial to Waveguide Adapter	1	-do-	-do-
7.	Power Meter	1	-do-	-do-

THEORY:

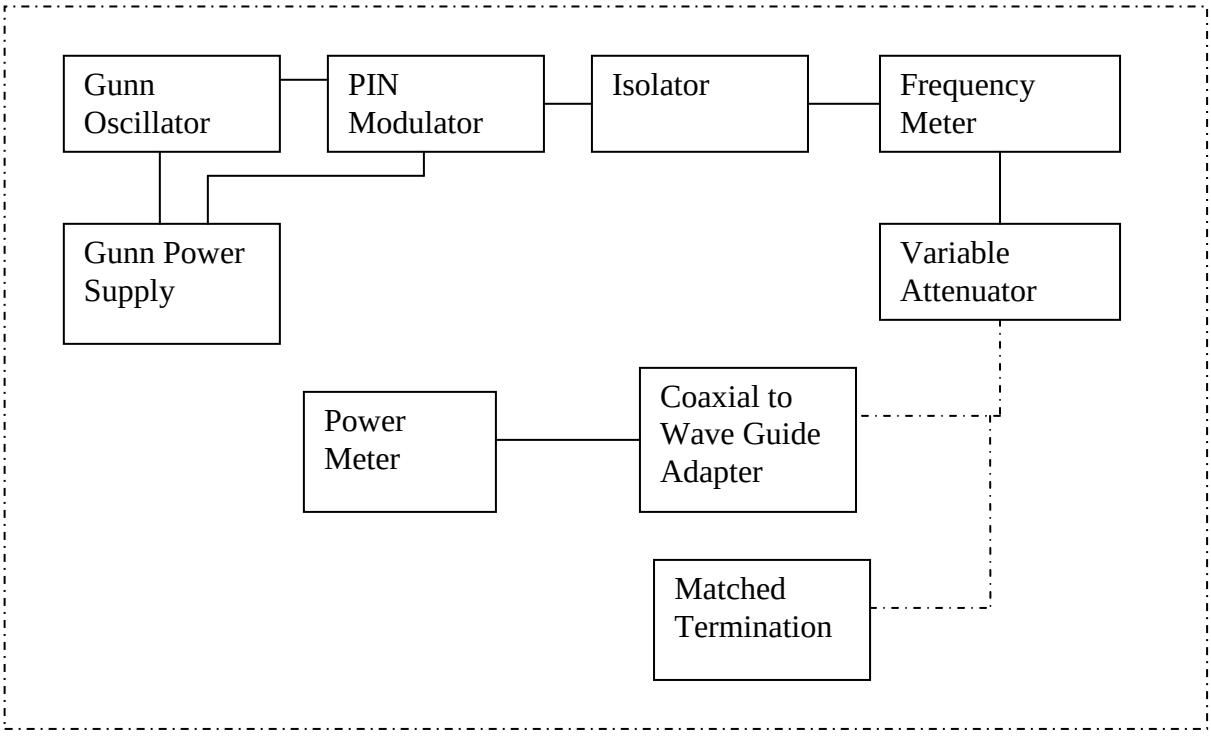
The Gunn Oscillator is based on negative differential conductivity effect in bulk semiconductors, which has two conduction bands minima separated by an energy gap (greater than thermal agitation energies). A disturbance at the cathode gives rise to high field region, which travels towards the anode. When this high field domain reaches the anode, it disappears and another domain is formed at the cathode and starts moving towards anode and so on the time required for domain to travel from cathode to anode (transit time) gives oscillation frequency.

In a Gunn Oscillator, the Gunn diode is placed in a resonant cavity. In this case the oscillation frequency is determined by cavity dimension than diode itself.

Although Gunn oscillator can be amplitude modulated with the bias voltage. We have used separate PIN modulator through PIN diode for square wave modulation.

A measure of the square wave modulation capability is the modulation depth i.e. the output ratio between, 'ON' and 'OFF'.

EXPERIMENTAL SETUP:



OBSEVATION TABLE (1): Gunn diode Characteristics

Sl. No.	Bias Voltage (volts)	Current (mA)
1	0	0
2	.5	…
3	1	…
…	…	…
20	…	…
21	10	…

OBSEVATION TABLE (2): Power Output vs. Frequency Plot

Sl. No. of Obs.	Freq. (GHz)	O/P power (mW)
1	..	
2	…	…
3	…	…
4	…	…
5	…	…

PROCEDURE:

1. Set the components and equipment as shown in the set up.
2. Set the variable attenuator for maximum attenuation.
3. Keep the control knob of Gunn Power Supply as below.

Meter Switch - OFF

Gunn Bias Knob - Fully anticlockwise

PIN bias Knob - Fully anticlockwise

PIN Mod frequency - Any position

4. Set the micrometer of Gunn Oscillator for required frequency of operation say 9 GHz.
5. Switch on the Gunn Power Supply and Cooling Fan.
6. Turn the meter switch of Gunn Power Supply to voltage position.
7. Change the Gunn Biasing in Steps of 0.5 V and record the corresponding current in observation table (read the Gunn bias and current in the panel meter of the Gunn Power Supply Unit). Maximum Gunn Bias Should be varied up to 10 V.
8. Draw the current – voltage characteristics curve and find the Threshold voltage V_{th}
9. Set the Gunn bias at 9 Volts. Referring the calibration chart of the Gunn Oscillator set the micrometer Screw for a frequency the X- Band. Tune the wave meter to get a dip in the power meter reading. Read the frequency of the microwave carrier from the wavemeter and record in the observation table II.
10. Mistune the wavemeter and read the power of the microwave signal and record in the observation table II.
11. Draw the power vs. frequency characteristics curve of the Gunn oscillator.
12. Draw the Conclusion.

Note:- Do not keep the Gunn Bias Knob at threshold position for more than 10-15 sec . Reading should be obtained as fast as possible. Otherwise due to excessive heating, Gunn diode may burn.

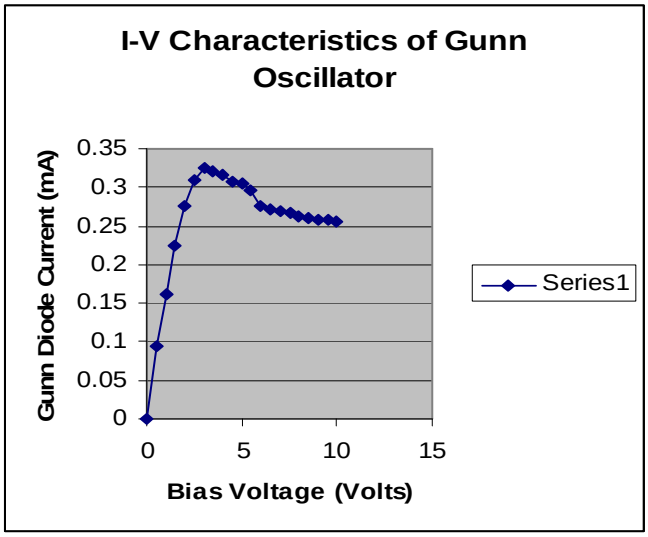


Fig.1: --a sample graph of I-V characteristics

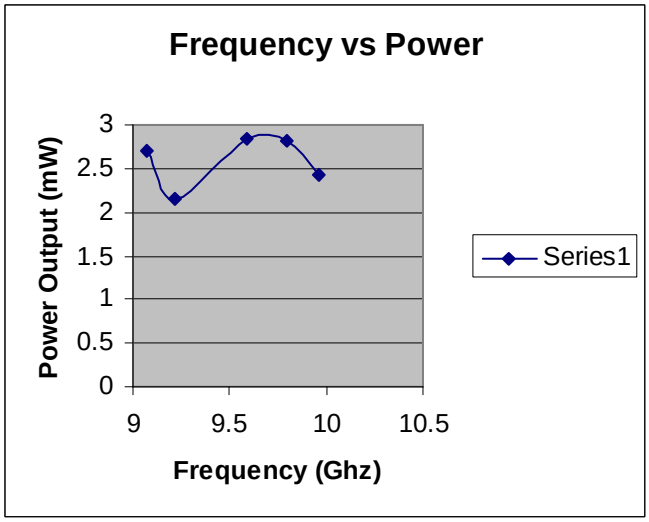


Fig.2: -- A sample graph of power vs. frequency characteristics.

CONCLUSION:

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Experiment No.: 5

AIM: Measurement of coupling and directivity of a Multihole Directional Coupler.

OBJECTIVES:

a. **To measure the main-line and auxiliary-line VSWR.**
b. **To measure the coupling factor and directivity.**

APPARATUS USED:

Sr. No.	Name of the equipment	Quantity	Range/Rating	Make
1.	Reflex Klystron/Gunn Oscillator	1	X – Band	SICO/ScienTech
2.	Klystron Power Supply/Gunn Power Supply	1	-do-	-do-
3.	Pin Modulator	1	-do-	-do-
4.	Isolator	1	-do-	-do-
5.	Variable Attenuator	1	-do-	-do-
6.	Frequency Meter	1	-do-	-do-
7.	Slotted Section	1	-do-	-do-
8.	Tunable Probe	1	-do-	-do-
9.	Detector Mount	1	-do-	-do-
10.	Matched Termination	1	-do-	-do-
11.	Multi-hole Directional	1	-do-	-do-
12.	Coupler	1	-do-	-do-
13.	VSWR Meter	1	-do-	-do-
14.	Movable Short	1	-do-	-do-
15.	CRO	1	-do-	-do-

THEORY:

A directional coupler is a device with which it is possible to measure the incident and reflected wave separately. It consists of two transmission line, the main arm and auxiliary arm, electronically coupled to each other. Refer to the fig. no. 1. The power entering port1 the main arm gets divided between port2 and 3 and almost no power comes out in port 4.

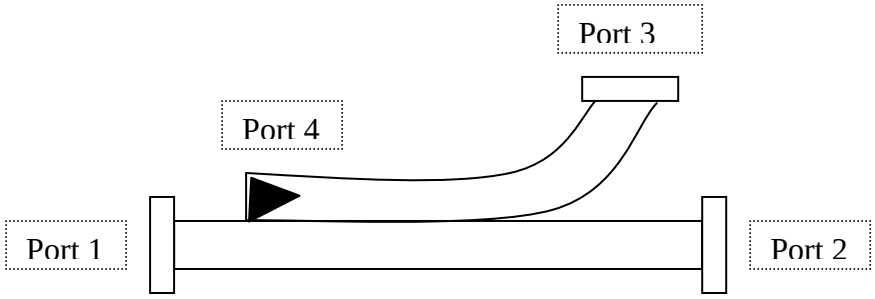

Fig. 1:---Directional Coupler

The coupling factor is defined as

Coupling (dB) = $10 \log_{10} [P_1/P_3]$ where port 2 is terminated,

Isolation (dB) = $10 \log_{10} [P_2/P_3]$ where P_1 is matched,

With built in termination and power is entering at port 1. The directivity of the coupler is a measure of separation between incident and the reflected wave. It is measured as the ratio of two power outputs from the auxiliary line when a given amount of power is successively applied to each terminal of the main lines with the port terminated by material loads.

Hence Directivity D (dB) = Isolation – Coupling = $10 \log_{10} [P_2/P_1]$.

Main line VSWR is SWR measured looking into the main line input terminal when the matched loads are placed at all other ports.

Auxiliary line VSWR is SWR measured in the Auxiliary line looking into the output terminal, when the matched loads are placed on other ports.

Main line insertion loss is the attenuation introduced in transmission line by insertion of coupler. It is defined as

Insertion Loss = 10 $\log_{10}$ [P_1/P_2] when power is entering at port 1.

Experimental Set Up

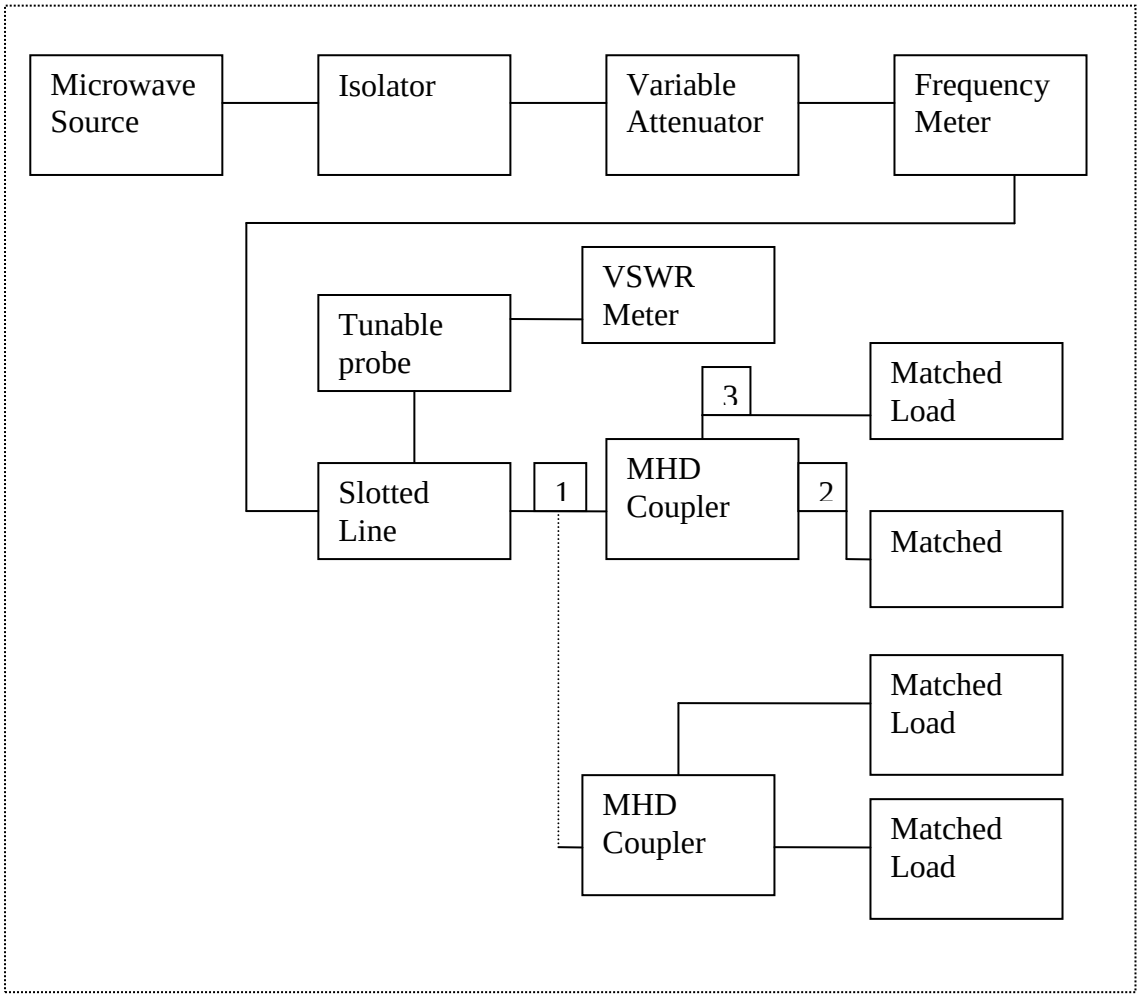

Fig.1: – Set Up for the measurements of VSWR of MHD Coupler

PROCEDURE:

A. MAIN LINE SWR MEASUREMENT

1. Set up the components and equipments as shown in fig. 1.
2. Energize the microwave Source for particular frequency operation as scribed. (Procedures given in the operation of Klystron and Gunn Oscillator).
3. Follow the procedure as described for VSWR measurement experiment (low and medium measurement).
4. Repeat the same for other frequencies.

B. AUXILLIARY LINE SWR MEASUREMENT

1. Set up the components and equipments as shown in fig. 1.
2. Energize the microwave Source for particular frequency operation as scribed operation of Klystron and Gunn Oscillator.
3. Measure SWR as described in the experiment of SWR measurement (low and medium SWR measurement).
4. Repeat the same for other frequencies.

C. MEASUREMENT OF COUPLING FACTOR, INSERTION LOSS

1. Set up the components and equipments as shown in fig. 1.
2. Energize the microwave Source for particular frequency operation as scribed operation of Klystron and Gunn Oscillator.
3. Remove the multihole directional coupler and connect the detector mount to the frequency meter. Tune the detector for the maximum output.
4. Set any reference level of power on the VSWR meter with the help of variable attenuator, gain control knob of VSWR meter, and note down the reading. (Reference level let it be X).
5. Insert the directional coupler as shown in second fig. with detector to the auxiliary port 3 and matched termination to port 2, without changing the position of variable attenuator and gain control knob of VSWR meter.
6. Note down the reading on VSWR meter on the scale with the help of range-dB switch if required. (Let it be Y)
7. Calculate coupling factor, which will be X-Y in dB.
8. Now carefully disconnect the detector from the auxiliary port 3 and match termination from port 2 without disturbing the set-up.
9. Connect the matched termination to the auxiliary port 3 and detector to port 2 and measure the reading on VSWR meter. Suppose it is Z.
10. Compute insertion loss X-Z in dB.
11. Repeat the step from 1 to 4.

12. Connect the directional coupler in the reverse direction, i.e. port 2 to frequency meter side, matched termination to port 1 and detector mount to port 3, without disturbing the position of the variable attenuator and gain control knob of VSWR meter.
13. Measure and note down the reading on VSWR meter, let it be Y_d.
14. Compute the directivity as Y- Y_d.
15. Repeat the same for other frequencies.

Observation Table:

Sl. No.	Frequency (GHz)	X (dB)	Y (dB)	Z (dB)	Y_d (dB)	Coupling Factor (X-Y) (dB)	Insertion Loss (X-Z) (dB)	Directivity (Y- Y_d) (dB)
1								
2								
3								
4								
5								

CONCLUSION: -

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Experiment No.: 6

EXPERIMENT NO: AIM: Study of **Magic Tee**

OBJECTIVES:

To Study isolation, coupling coefficients and input VSWRs of an E-H plane tee or magic tee

APPARATUS USED:

Sr. No.	Name of the equipment	Quantity	Range/Rating	Make
1.	Reflex Klystron/Gunn	1	X – Band	SICO/ScienTech
2.	Oscillator	1	-do-	-do-
3.	Klystron Power Supply/Gunn	1	-do-	-do-
4.	Power Supply	1	-do-	-do-
5.	Pin Modulator	1	-do-	-do-
6.	Isolator	1	-do-	-do-
7.	Variable Attenuator	1	-do-	-do-
8.	Frequency Meter	1	-do-	-do-
9.	Slotted Section	1	-do-	-do-
10.	Tunable Probe	1	-do-	-do-
11.	Detector Mount	2	-do-	-do-
12.	Matched Termination	1	-do-	-do-
13.	Magic Tee	1	-do-	-do-
14.	VSWR Meter	1	-do-	-do-
15.	Movable Short	1	-do-	-do-
	CRO			

THEORY:

The device magic Tee is a combination of the E-plane and H-plane Tee. Arm3, the H-arm forms an H-plane Tee and the E-arm forms an E-plane Tee in combination with arm 1 and 2 a side or collinear arms. If power is fed into arm 3 (H-arm) the electric field divides equally between arm 1 and 2 in the same phase, and no electric field exists in arm 4. Reciprocity demands no coupling in port 3 (H-arm). If power is fed in arm 4 (E-arm), it divides equally

into arm 1 and 2 but out of phase with no power to arm 3. Further, if the power is fed from arm 1 and 2, it is added in arm 3 (H-arm), and it is subtracted in E-arm, i.e. arm 4.

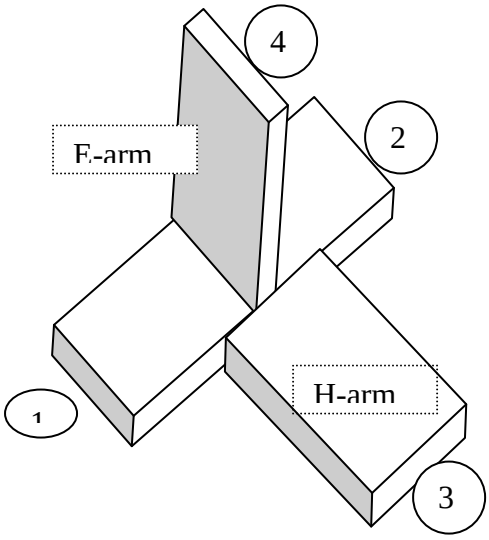

Fig:---- Magic Tee

The basic parameters to be measured for Magic Tee are defined below

A. INPUT VSWR

Value of SWR corresponding to each port, as a load to the line while other ports are terminated in matched load is determined.

B. ISOLATION

The isolation between E and H arms is defined as the ratio of the power supplied by the matched generator connected to the E-arm (port 4), to the power detected in H- arm (port 3) by a matched detector when collinear arms (1 and 2) are terminated in matched loads. It is expressed in dB.

Hence, $I_{34} = 10 \log_{10} [P_4/P_3]$

P_4 : Power incident in port 4 (E- arm)

P_3 : Power detected in port 3 (H- arm)

Similarly isolation between other ports may also be defined and measured.

C.COUPLING COEFFICIENT

The voltage coupling coefficient from arm I to arm j is defined as

$C_{ij} = 10^{-\alpha/20}$

Where α is the attenuation in dB when i is the input and j is the output arm.

Thus α (dB) = $10 \log_{10} [P_i/P_j]$

Where P_i is the power delivered to i arm by a matched generator and P_j is power detected by a matched detector in j arm.

In case of magic tee, there are 12 coupling constants, one for each of the arms as an input to each of the other three arms as an output. However, if we have a perfectly matched detector and generator, $C_{ij} = C_{ji}$ and the reciprocity desires $C_{12} = C_{21}$, $C_{32} = C_{31}$ and $C_{41} = C_{42}$.

EXPERIMENTAL SET UP

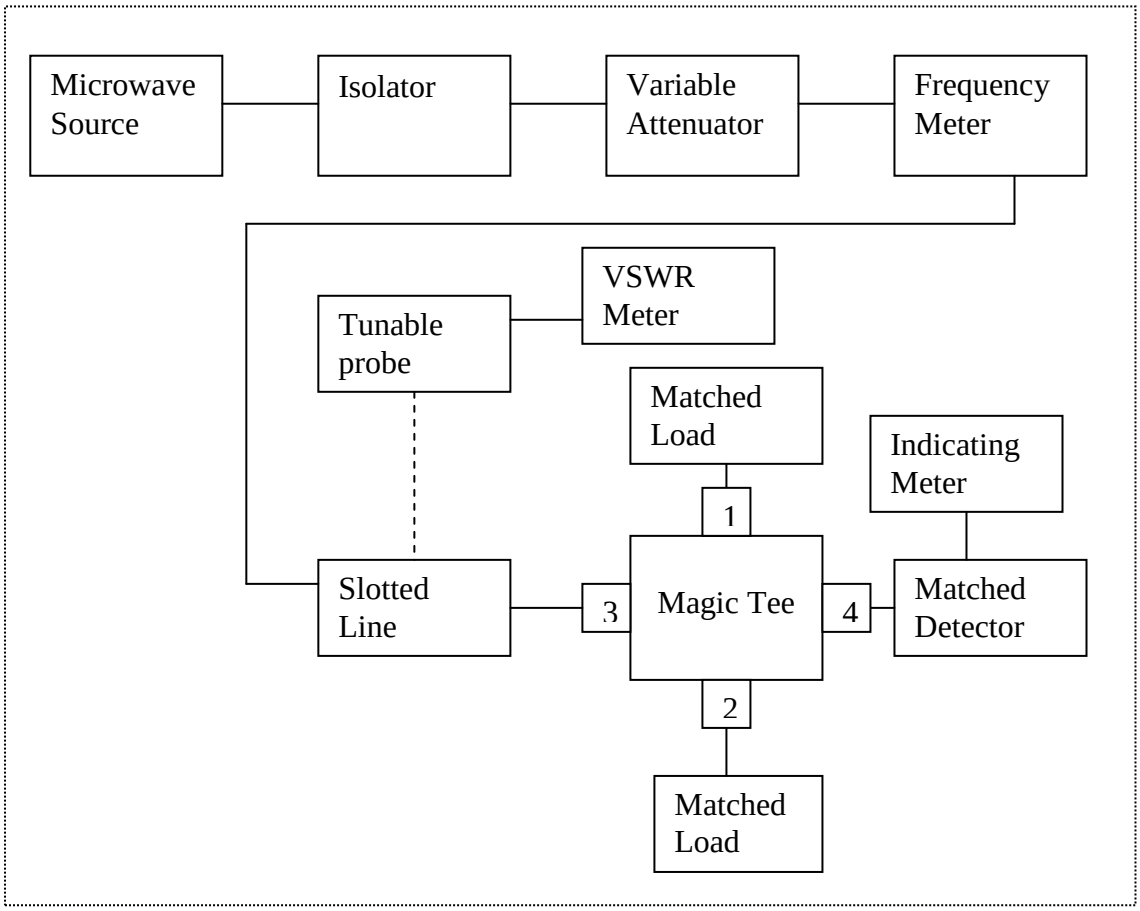

Fig. 2. Setup for the study of Magic Tee

PROCEDURE

1. Assemble the set up as shown in the figure without the magic tee.
2. Carefully remove the slotted section probe from the guide.
3. Energize the power source and adjust it for maximum power indication on SWR meter.
4. Adjust the coarse and fine control of the VSWR meter for reasonable power level say 20 dB and record this power level in the table as initial power
5. Carefully remove the detector set up and insert magic tee as shown in the figure and connect the detector on one of the ports and terminate other ports with matched loads.
6. Determine the attenuation and hence isolation in decibels by noting the change in the output level on the detector.
7. Reverse terminals one by one, connecting one arm to the generator, other to the detector and rest terminated in matched loads and record various isolation parameters in the observation table.
8. Determine coupling coefficients knowing attenuation in steps 6 and 7.
9. Insert probe in the slotted section and terminate slotted section in one of the arms of the tee and determine input VSWRs following the procedure of VSWR measurement.
10. Repeat step 9 each time for all other three ports taken as input arm and record in Table 2.

Observation table:1

Sl.No.	Orientation of Magic tee		VSWR /Power meter reading (dB/mW)		Isolation (dB)	Couplings coefficient
	Input arm	output arm	initial	final		
1.	3	1	20 dB	23.8	I_{31} = 3.8	C_{31} = 0.647
		2		23.6	I_{32} = 3.6	C_{32} = 0.661
		4		beyond 60 dB	I_{34} = more than 31 dB .	C_{34} =
2.	4	1	20 dB		I_{41} =	C_{41} =
		2			I_{42} =	C_{42} =
		3			I_{43} =	C_{43} =
3.	1	3	20 dB		I_{13} =	C_{13} =
		4			I_{14} =	C_{14} =
		2			I_{12} =	C_{12} =
4.	2	1	20 dB		I_{21} =	C_{21} =
		3			I_{23} =	C_{23} =
		4			I_{24} =	C_{24} =

___(One set of observation is given in the table)

Observation table 2

Sl. No.	Input arm	VSWR
1	1. Collinear arm	
2	2. Collinear arm	
3	3. H-arm	
4	4. E-arm	

CONCLUSION:

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Experiment No.: 8

AIM: Measurement of Dielectric Constant using wave-guide test Bench.

OBJECTIVE: To measure the Dielectric Constant of a given Dielectric sample with the help of microwave test bench.

APPARATUS USED:

Sr. No.	Name of the equipment	Quantity	Range/Rating	Make
1.	Reflex Klystron/Gunn	1	X – Band	SICO/ScienTech
2.	Oscillator	1	-do-	-do-
3.	Klystron Power Supply/Gunn	1	-do-	-do-
4.	Power Supply	1	-do-	-do-
5.	Pin Modulator	1	-do-	-do-
6.	Isolator	1	-do-	-do-
7.	Variable Attenuator	1	-do-	-do-
8.	Frequency Meter	1	-do-	-do-
9.	Slotted Section	1	-do-	-do-
10.	Tunable Probe	1	-do-	-do-
11.	VSWR Meter	1	-do-	-do-
12.	Movable Short	3	---	-do-
	Dielectric Sample			

Theory

In the wave guide method, a rectangular waveguide terminated by metal short acts as short circuit is connected to the output end of the slotted line. The voltage minima d_{1min} is located. The dielectric under test is shaped so as to fit into the waveguide. The sample of thickness t_1 is fitted into the waveguide end and is backed by a short circuit metal plate. The new voltage minimum d_{2min} is located. By using the impedance relation

$$Z_d \tan(\beta_d d_{1min}) = - Z_o \tan(\beta d_{2min}), \qquad \text{----------(1)}$$

The following transcendental equation can be derived:

$$\tan(\beta_d t_1)/ \beta_d t_1 = \tan[\beta(\Delta_1 + t_1)]/ \beta t_1, \qquad \text{----------(2)}$$

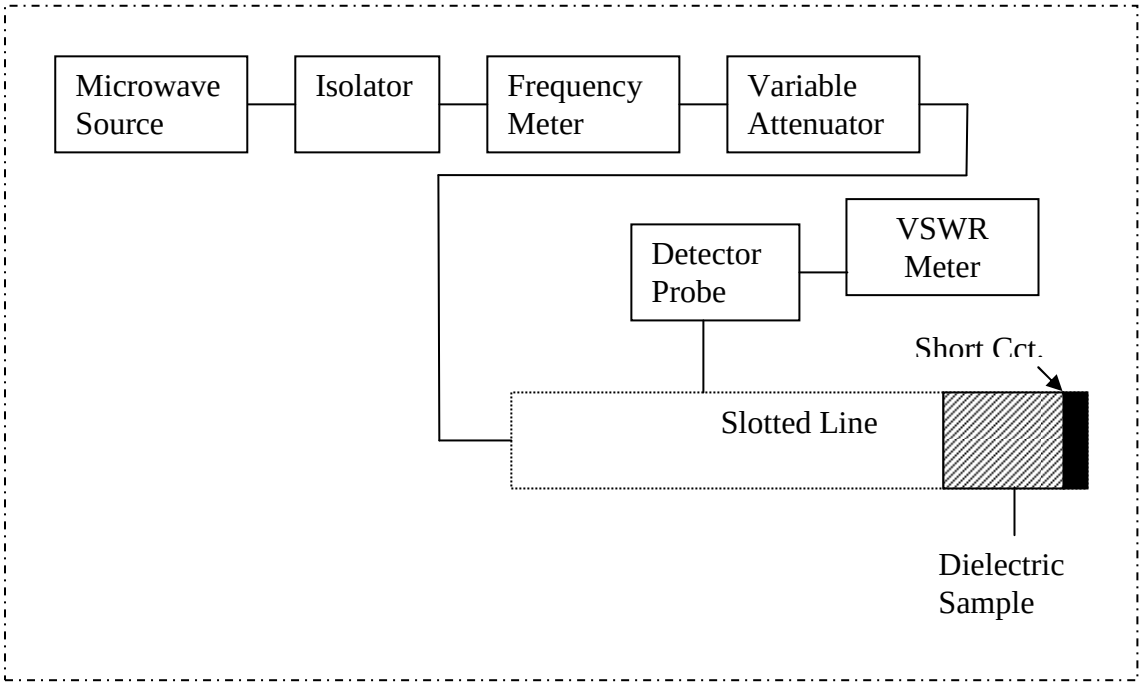
where $\Delta_1 = d_{1min} - d_{2min}$ is the shift in the position of minimum; $\beta = 2\pi/\lambda_g$ and β_d denote the phase constants in the empty guide and in the dielectric, respectively. Equation (2) is solved for $\beta_d t_1$ and the dielectric constant of the sample is calculated from the relation

$$\varepsilon_r = \{ (a/\pi)^2 (\beta_d t_1/t_1)^2 +1\}/\{(2a/\lambda_g)^2 + 1\}, \qquad \text{----------(3)}$$

where a = broad wall dimension of the waveguide.

The solution of (3) gives us multiple roots. The measurement is repeated with a second and third sample of thickness t_2 and t_3, and β_d is determined. The correct solution is the common to the three measurements. The method is applicable for dielectrics with very low value of tanδ. The airgap between the shorting plate and the sample should be reduced to the minimum to obtain ε_r tanδ accurately.

Experimental Setup:



Procedure:

1. Connect the equipment as shown in the set up
2. Energize the microwave source and obtain the suitable power level in the indicating meter.
3. With no sample in the short circuited line, find the first position of voltage minima d_{1min} , and record in the observation table with the help of slotted section and probe.
4. Measure the guide wave length λ_g by measuring the distance between two successive minima in the slotted line.
5. Remove the short circuit, insert a sample dielectric and replace the short circuit in such a manner that it touches the end of the sample.
6. Measure d_{2min} , the first position of minima in the slotted line.
7. Measure VSWR in the slotted line.
8. Repeat steps (3) to (6) with sample having different lengths.
9. Compute the dielectric constant of the given sample.

Observation table:

(i) Wave guide dimension a = ---------- cm
(ii) Cut-off wavelength $\lambda_c = 2a$ = ----------cm
(iii) Frequency of operation = ----------GHz
(iv) Temperature = ----------^oC
(v) VSWR, *S* =----------(with sample)

Sample	Thickness (t_1)	position of standing wave minima		tan [β (Δ_1 + t_1)]/ βt_1	(tanX)/X	value of X
		Wave guide Unload (d_{1min})	Wave guide loaded With Dielectric (d_{2min})			
1						X_1 =
						X_2 =
						X_3 =
2						X_1 =
						X_2 =
						X_3 =
3						X_1 =
						X_2 =
						X_3 =

Calculation:

CONCLUSION: -